HAWAII BLOCK DIAGRAM

SYSTEM PAGE REF.

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05. CPU(3)_+VCCCORE
06. CPU(4)_+VCCGT
07. CPU(5)_+VDDQ/IO/SA
08. CPU(6)_CPU GND
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24. PCH(5)_CLK / RTC/ CSI-2
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32. RST_Reset Circuit
36. Codec / Jack / SpK / DMIC
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44. Debug CONN
45. LCM_EDP
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51. SSD NGFF.
52. USB 3.0 Port
53. WLAN / WiGig / BT NGFF.
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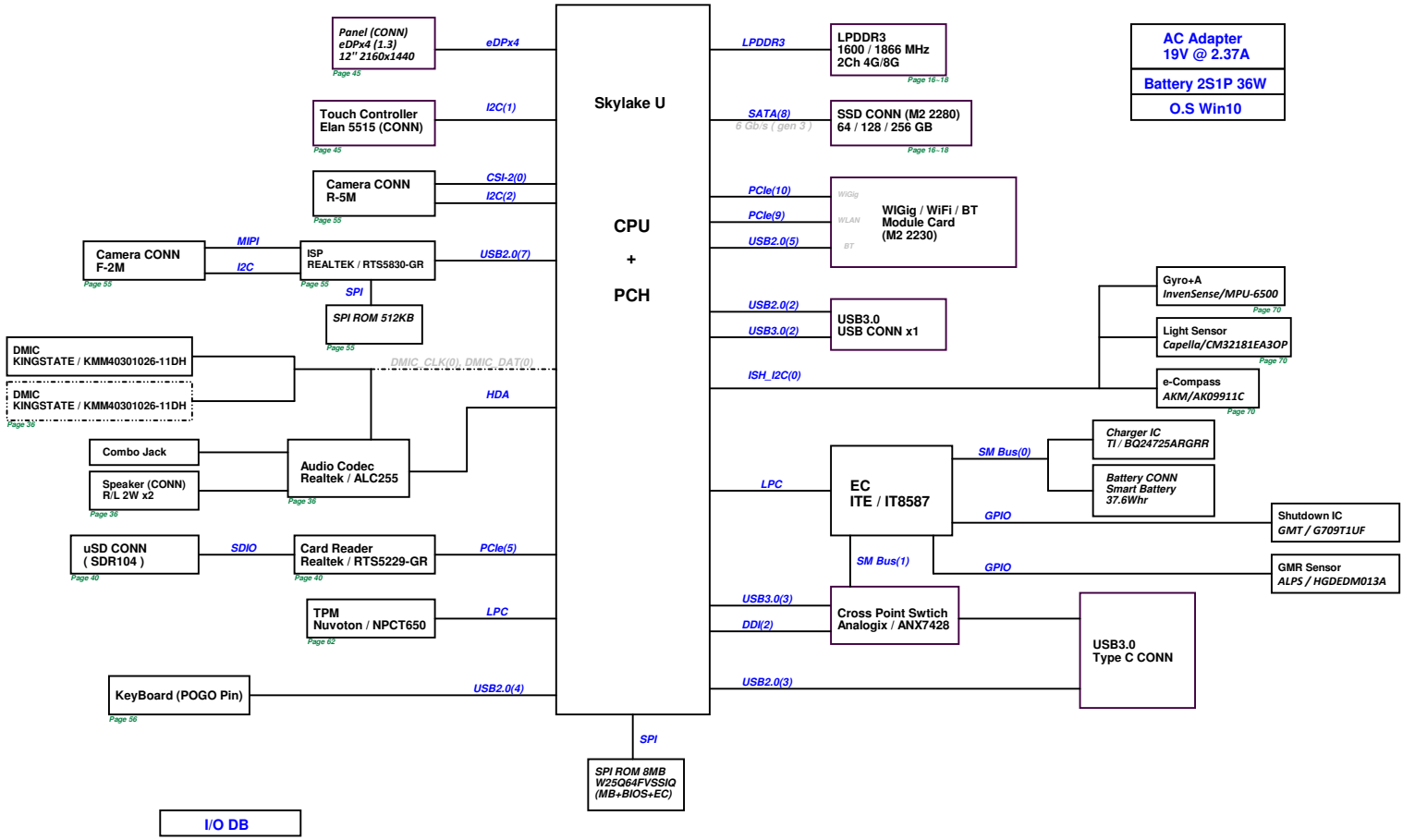
56. IO CONN / POGO PIN
57. Discharge
60. DC_DC / BAT CONN
62. TPM
68. BYPASS EC SEQUENCE
70. Sensor / GMR
80_POWER_VCORE for U22
81_POWER_SYSTEM
82_POWER_+1.0VSUS
83_POWER_ DDR & VTT_UMA
84_POWER_1.8VSUS
88_POWER_CHARGER
89_POWER_ AC_PD_WC Input
90_POWER_DETECT
91_POWER_LOAD SWITCH
92_POWER_PROTECT
93_POWER_SIGNAL
94_POWER_FLOWCHART
95_USB_TYPE-C ANX7428
96_USB Type-C Receptacle
A01. Power Tree



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : Block Diagram
NBRDC4W3
Engineer: Willy_Liao
Size: D
Project Name: HAWAII
Rev: 0.0
Date: Thursday, March 31, 2016
Sheet 1 of 100

EC GPIO	Use As	Signal Name	EC GPIO	Use As	Signal Name

EC GPIO	Use As	Signal Name

EC GPIO	Use As	Signal Name

SKU Table (B2 build)

Mount Table

Optional	Mount?
/1st_SSD	V
/2nd_SSD	X
/MEM-CH1	V
/MEM-CH2	V
/E_SENSOR_HUB	V
/TPM	V
/Debug	V
/NON-IOAC	V
/USBSLP	V
/IOAC	X
/SEQS_EC	X
/BYPAS_EC	V
/ADSP	V
/RTL	X

+VCCIO +VCCIO [7,9,91]
+VCCST_CPU +VCCST_CPU [5,7,9,25,32]
+VCCSTG +VCCSTG [5,7]
+3VS +3VS [4,20,21,22,23,24,30,32,36,40,41,44,45,50,51,53,55,56,57,62,70,91,92]

SKYLAKE-U symbol RevV0.53 #545316 / Ballout_Rev0_71 #543787 / PEGA local PN is 4201-0062000

U0301A

Remove DDI1 Port : HDMI

DDI Port 2: USB_TYPE C_DP

DDI1_TXN[0] E55
DDI1_TXP[0] F55
DDI1_TXN[1] E58
DDI1_TXP[1] F58
DDI1_TXN[2] F53
DDI1_TXP[2] G53
DDI1_TXN[3] F56
DDI1_TXP[3] G56

[95] DDI2_TXN0 C50
[95] DDI2_TXP0 D50
[95] DDI2_TXN1 C52
[95] DDI2_TXP1 D52
[95] DDI2_TXN2 A50
[95] DDI2_TXP2 B50
[95] DDI2_TXN3 D51
[95] DDI2_TXP3 C51

DDI2_TXN[0] C50
DDI2_TXP[0] D50
DDI2_TXN[1] C52
DDI2_TXP[1] D52
DDI2_TXN[2] A50
DDI2_TXP[2] B50
DDI2_TXN[3] D51
DDI2_TXP[3] C51

DDI
EDP
DISPLAY SIDEBANDS

GPP_E18/DDPB_CTRLCLK L13
GPP_E19/DDPB_CTRLDATA L12
DDPC_CTRLCLK N7
DDPC_CTRLDATA N8
GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA
N11
[56] TP_RST N12
GPP_E22
GPP_E23
+VCCIO R0301 1 1% 2 24.9Ohm DP_COMP E52
tx_r0402
eDP_RCOMP

940432
01T10000015

EDP_TXN[0] C47
EDP_TXP[0] C46
EDP_TXN[1] D46
EDP_TXP[1] C45
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_TXN0 [45]
EDP_TXP0 [45]
EDP_TXN1 [45]
EDP_TXP1 [45]
EDP_TXN2 [45]
EDP_TXP2 [45]
EDP_TXN3 [45]
EDP_TXP3 [45]

eDP x 4
-- WQHD 4 Lane
-- FHD 2 Lane

EDP_AUXN E45
EDP_AUXP F45
EDP_AUXN [45]
EDP_AUXP [45]
AUX For eDP

EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
RSVD_1 G46
RSVD_2 F46
No Connect
543016 page 824
DDI2_AUXN [95]
DDI2_AUXP [95]

GPP_E13/DDPB_HPD0 L9 DDI1_HPD
GPP_E14/DDPC_HPD1 L7 DDI2_HPD
GPP_E15/DDPD_HPD2 L6 EXT_SMI# R R0302 1 2 0Ohm tx_r0402 EXT_SMI#
GPP_E16/DDPE_HPD3 N9 EXT_SCI# R R0303 1 2 0Ohm tx_r0402 EXT_SCI#
GPP_E17/EDP_HPD L10 eDP_HPD
DDI2_HPD [95]
EXT_SMI# [30,44]
EXT_SCI# [30]
eDP_HPD [45]

eDP_BKLTEN R12
eDP_BKLTCTL R11
eDP_VDDEN U13
LCD_BKLTEN_PCH [21,45]
LCD_BL_PWM_PCH [45]
EDP_VDD_EN [45]

DDPC_CTRLDATA R0305 1 2 2.2kOHM tx_r0402
DDPC_CTRLCLK R0340 1 2 2.2kOHM tx_r0402
+3VS
DDPB_CTRLDATA
DDPC_CTRLDATA
DDPD_CTRLDATA
- Internal weak pull down 20k ohm
- 0 : port is not detected
1 : port is detected

EXT_SCI# R0307 1 2 10KOHM tx_r0402
EXT_SMI# R0308 1 2 10KOHM tx_r0402
+3VS

eDP_HPD R0344 10KOhm tx_r0402 @ R0346 100KOHM tx_r0402
DDI1_HPD R0343 10KOhm tx_r0402 @ R0342 20KOhm tx_r0402
DDI2_HPD R0345 10KOhm tx_r0402 @ R0337 100KOHM tx_r0402
+3VS
DDPB_HPD0
DDPC_HPD1
DP: 100Kohm pull down on PCH Side
HDMI: 20Kohm pull down

+VCCST_CPU
+VCCSTG
141024 follow PDG V1.0 Table 10-4
Rpu = 1K ohm 5%
Rs = 500 ohm 5%
Closeer EC
+VCCST_CPU
R0311 1KOhm tx_r0402
R0312 1KOhm tx_r0402 5%
R0313 49.9Ohm tx_r0402 1%

[30] H_PECI_EC
[32] H_THRMTRIP#
H_PROCHOT#
R0314 1 1% 2 499Ohm tx_r0402
R0315 1 2 43Ohm tx_r0402
SP0301 1 2
TP_CATERR# R D63
H_PECI A54
H_PROCHOT# R C65
H_THRMTRIP# R C63
T0306 1 SKTOCC# A65

Remove XDP_BPM#

+3VS
R9617 10KOhm tx_r0402
[56] TP_INT

T0311 1 CPU_GP0 A6
TP_INT A7
T0313 1 CPU_GP2 BA5
T0314 1 CPU_GP3 AY5

R0316 1 1% 2 49.9Ohm tx_r0402 CPU_POPIRCOMP AT16
R0317 1 1% 2 49.9Ohm tx_r0402 PCH_POPIRCOMP AU16
R0318 1 1% 2 49.9Ohm tx_r0402 EDRAM_OPIO_RCOMP H66
R0319 1 1% 2 49.9Ohm tx_r0402 EOPIO_RCOMP H65

U0301D

CATERR# D63
PECI A54
PROCHOT# C65
THERMTRIP# C63
SKTOCC# A65
CPU MISC
BPM#[0] C55
BPM#[1] D55
BPM#[2] B64
BPM#[3] C56
GPP_E3/CPU_GP0 A6
GPP_E7/CPU_GP1 A7
GPP_B3/CPU_GP2 BA5
GPP_B4/CPU_GP3 AY5
PROC_POPIRCOMP AT16
PCH_OPIRCOMP AU16
OPCE_RCOMP H66
OPC_RCOMP H65

940432
01T10000015

JTAG
PROC_TCK B61
PROC_TDI D60
PROC_TDO A61
PROC_TMS C60
PROC_TRST# B59
PCH_JTAG_TCK B56
PCH_JTAG_TDI D59
PCH_JTAG_TDO A56
PCH_JTAG_TMS C59
PCH_TRST# C61
JTAGX A59

XDP_TCLK
XDP_TDI_CPU
XDP_TDO_CPU
XDP_TMS_CPU
XDP_TRST_CPU_N
PCH_JTAG_TCLK 1 T0315
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_TRST_CPU_N
XDP_TCLK_JTAGX

XDP Less Default Mount
+VCCSTG
PCH_JTAG_TDO XDP_TDO_CPU R0323 2 1 51Ohm tx_r0402
PCH_JTAG_TMS XDP_TMS_CPU 1 T0316
PCH_TRST_CPU_N XDP_TRST_CPU_N 1 T0317
PCH_JTAG_TDI XDP_TDI_CPU 1 T0318
XDP_TCLK_JTAGX XDP_TCLK R0324 2 1 51Ohm tx_r0402
XDP Less Default Mount
Modify to XDP less

[80] VR_HOT#
R0320 1 @ 2 0Ohm tx_r0402_0ohm
H_PROCHOT#
R1.1
R0341由EC control 觸發時的對地電阻也是要介於 70-200 ohm
(depends on under-shoot measurement result),預留0ohm是調整空間
R0341 0Ohm tx_r0402_0ohm
Q0301 NX7002AK
THRO_CPU [30]

SKYLAKE
PROC_PREQ#
PROC_PRDY#
CFG[3]
ITP_PMODE
SYS_RESET#
RSMRST#
SPIO_IO2
PCH_TRST#
PROC_TDO
PROC_TMS
PROC_TRST#
PROC_TDI
PROC_TCK
JTAGX
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_JTAG_TCK
PCH_JTAG_TDI
TP
R3
R1 51 Ohm GND
R2 51 Ohm VCCSTG (or Equivalent)

-- Stubs on JTAG nets should not more than 200ps
-- R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
-- Place Test point pads on Secondary side
-- Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPIO_IO2 VCCOBS_AB (PCH V1.0 A), GND pins (2)
-- TP should be placed to within 250ps of the respetive Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
-- TP = Test Point Pad (size - 18 mil min, 25 mil preferred) The pad side must meet the industrial standard of Boundary Scan Test.

Figure 44-6. Connector Less Routing Topology

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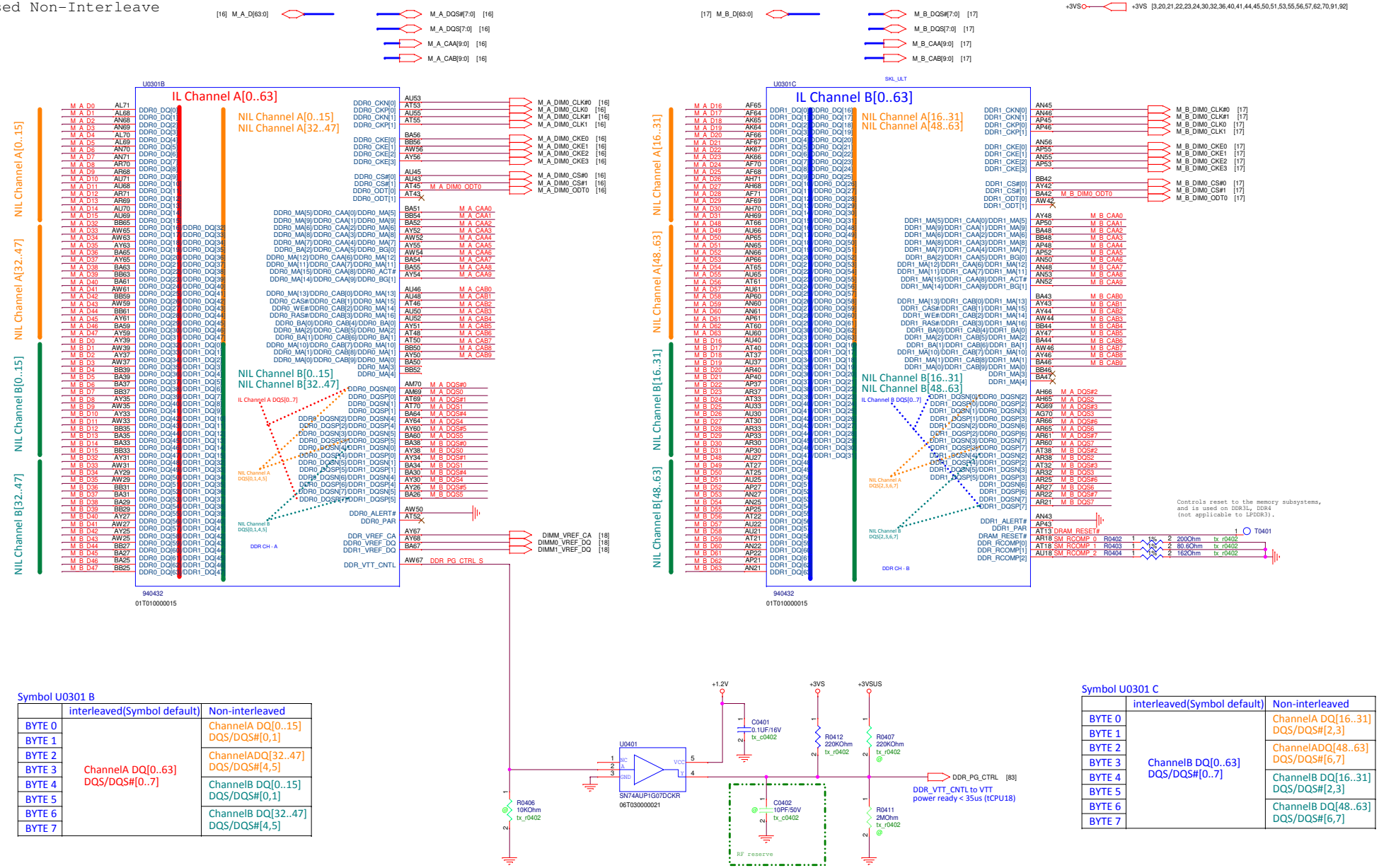
Title : CPU(1)_DDI/eDP
Engineer: Willy_Liao
Size C
Project Name HAWAII
Rev 0.0
Date: Thursday, March 31, 2016
Sheet 3 of 100

T25S used Non-Interleave



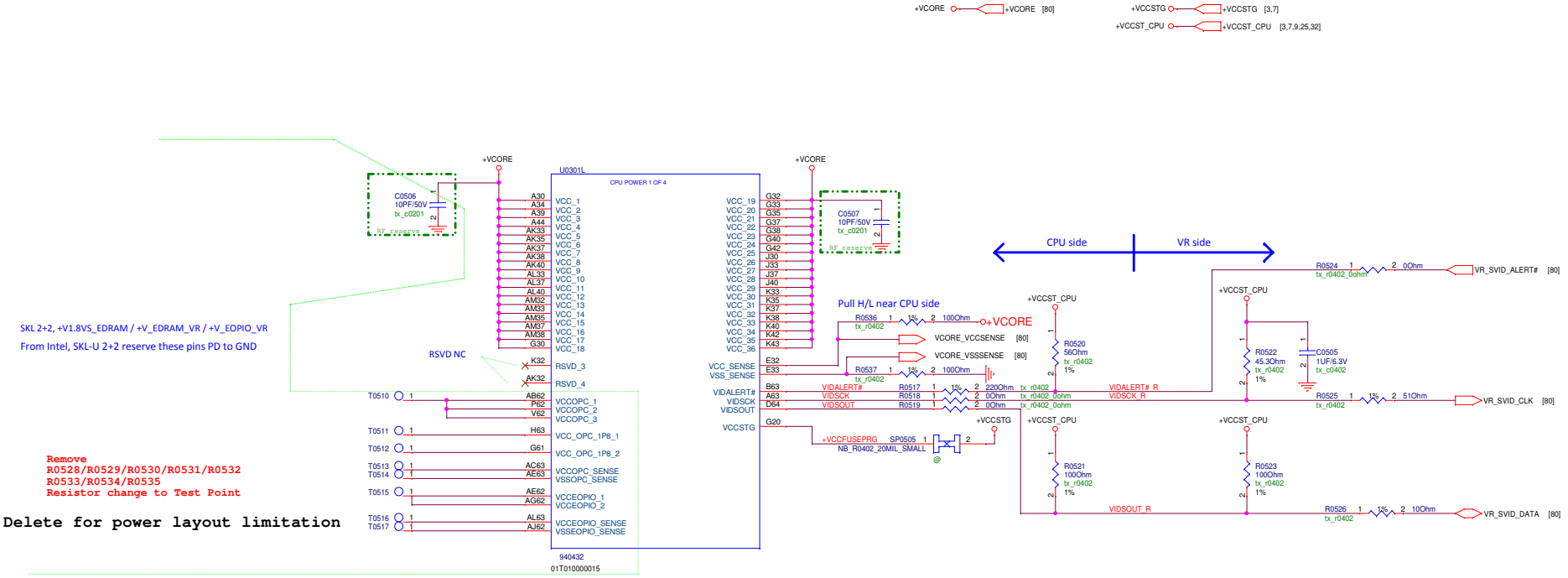
Symbol U0301 B

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelA DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[0..15] DQS/DQS#[0,1]
BYTE 1		
BYTE 2		ChannelADQ[32..47] DQS/DQS#[4,5]
BYTE 3		
BYTE 4		ChannelB DQ[0..15] DQS/DQS#[0,1]
BYTE 5		
BYTE 6		ChannelB DQ[32..47] DQS/DQS#[4,5]
BYTE 7		

Symbol U0301 C

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelB DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[16..31] DQS/DQS#[2,3]
BYTE 1		
BYTE 2		ChannelADQ[48..63] DQS/DQS#[6,7]
BYTE 3		
BYTE 4		ChannelB DQ[16..31] DQS/DQS#[2,3]
BYTE 5		
BYTE 6		ChannelB DQ[48..63] DQS/DQS#[6,7]
BYTE 7		

PEGATRON Title : CPU(2)_DDR3L
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Willy_Liao
BG1-NB4
Size C | Project Name HAWAII | Rev 0.0
Date: Thursday, March 31, 2016 | Sheet 4 of 100



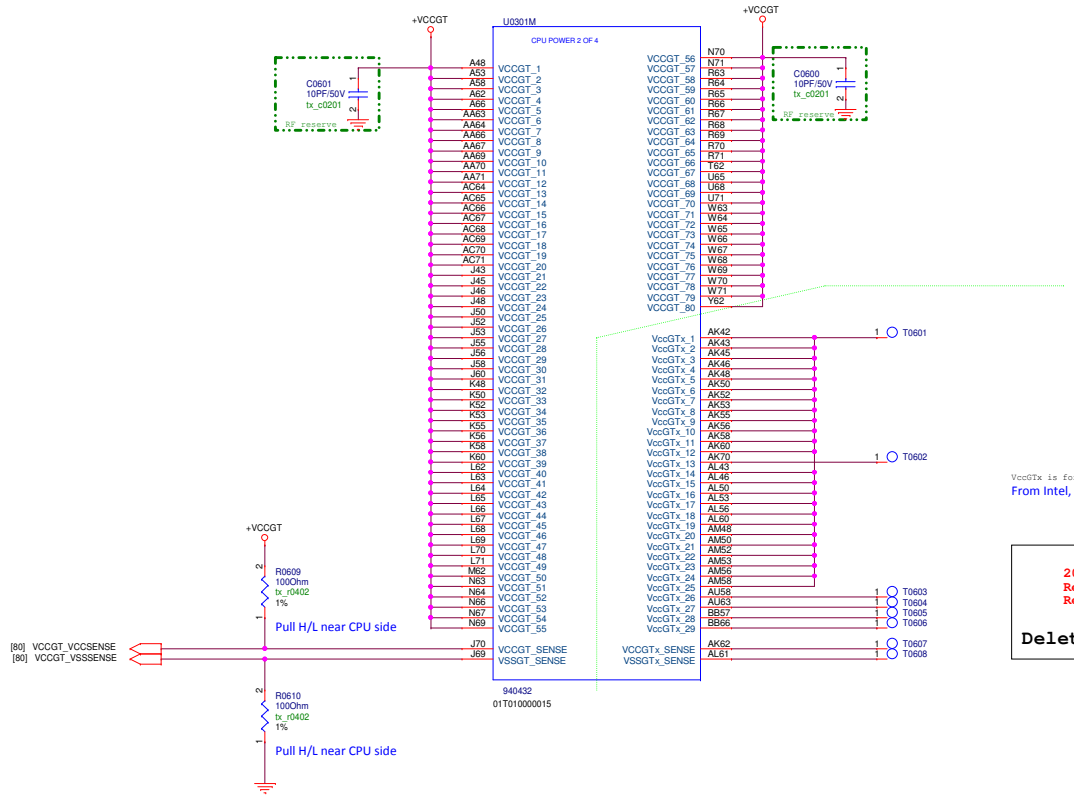
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : CPU(3)_+VCCCORE

Engineer: Willy_Liao

Size	Project Name	Rev
C	HAWAII	0.0

Date: Thursday, March 31, 2016 Sheet 5 of 100



+VCCGT +VCCGT [80]

VccGTx is for 2+3e.

From Intel, SKL-U 2+2 reserve these pins PD to GND

2015/01/20
Remove R0601-R0608
Resistor change to Test Point

Delete for power layout limitation

PEGATRON Title : CPU(4)_+VCCGT

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Willy_Liao

Size	Project Name	Rev
C	HAWAII	0.0

Date: Thursday, March 31, 2016 Sheet 6 of 100

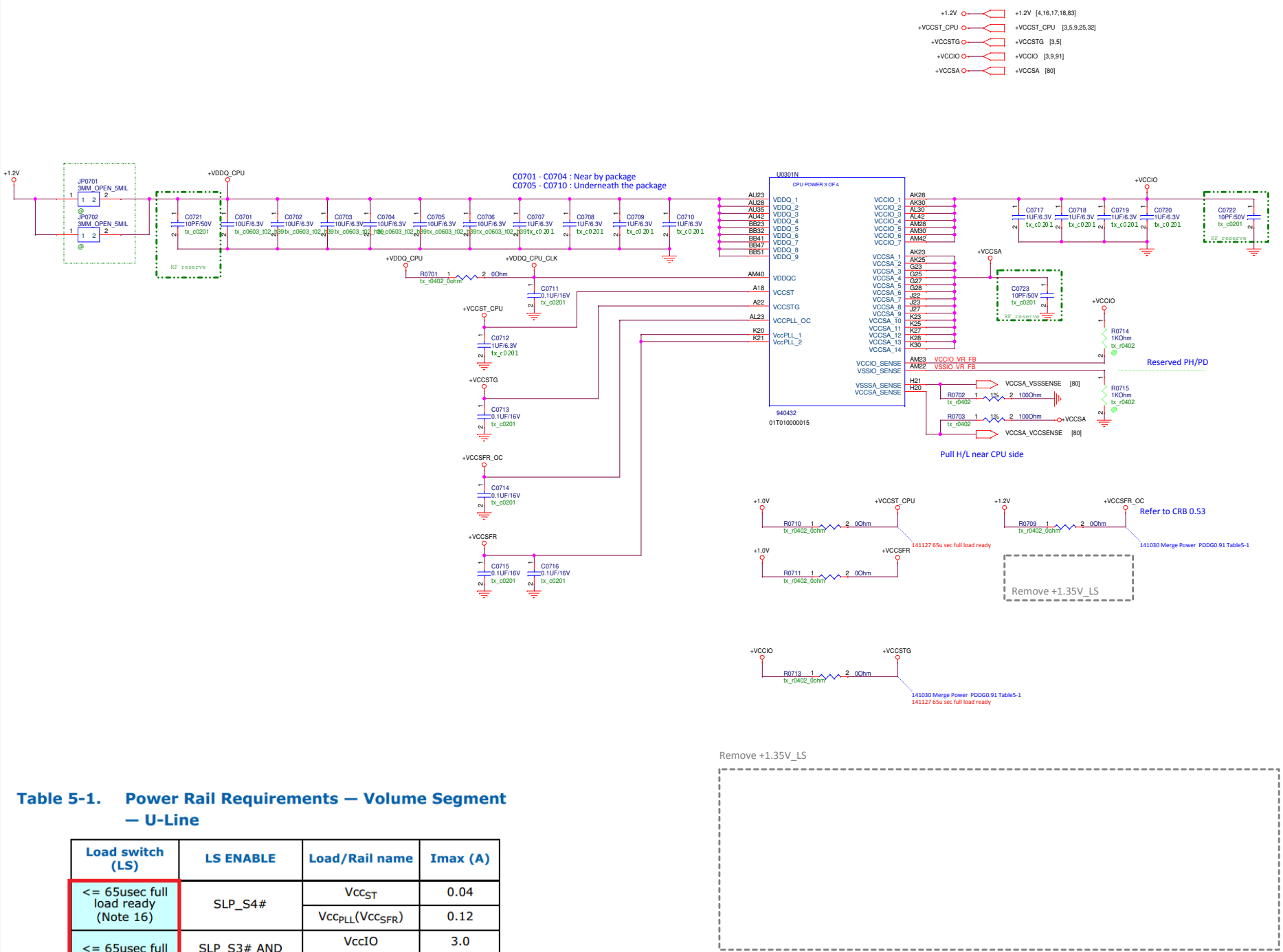
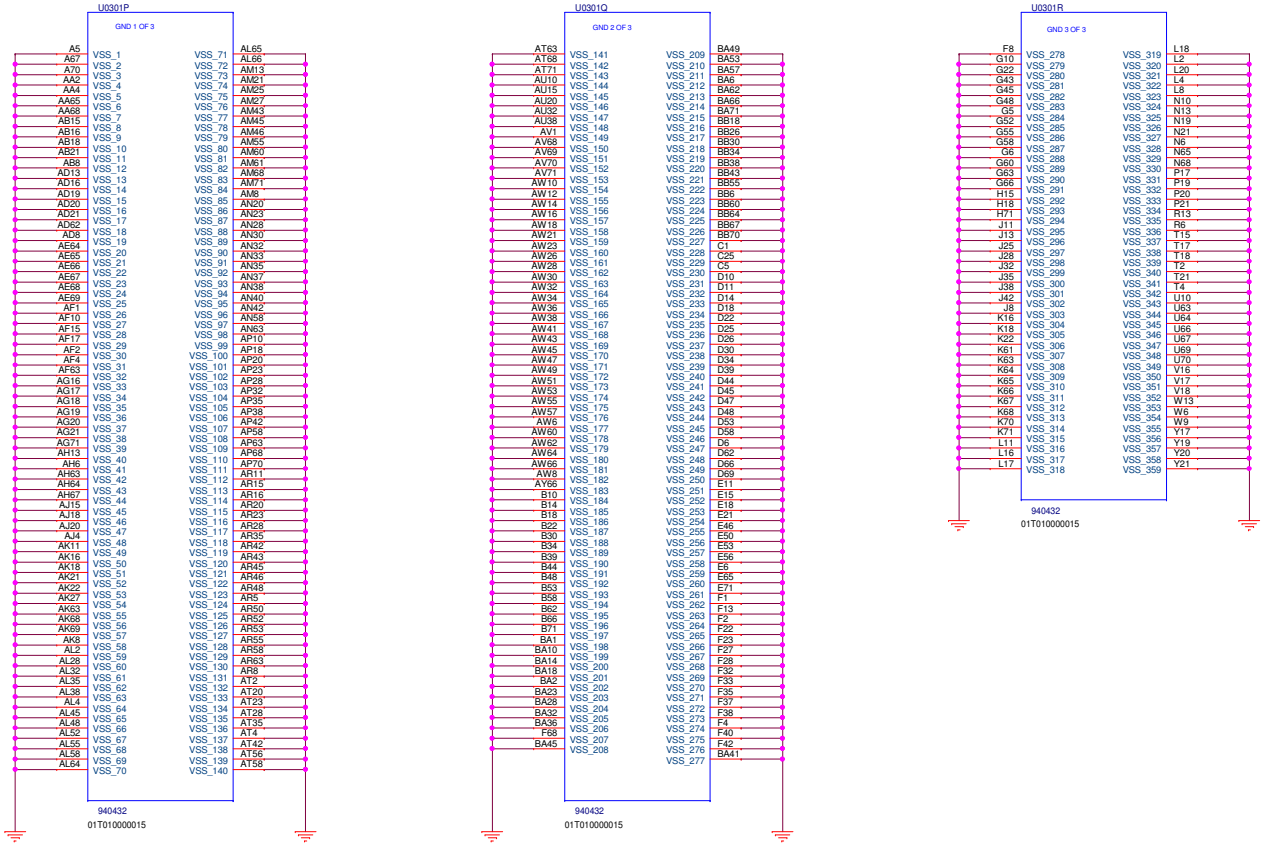


Table 5-1. Power Rail Requirements — Volume Segment — U-Line

Load switch (LS)	LS ENABLE	Load/Rail name	Imax (A)
<= 65usec full load ready (Note 16)	SLP_S4#	Vcc_{ST}	0.04
		Vcc_{PLL}(Vcc_{SFR})	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	VccIO	3.0
		Vcc_{STG}	0.04

16. VCCST ramp time can potentially be slowed than listed, depending on platform design. However, all timings documented in the PSS chapter must be met, specifically Tcpu_04

reference 543977_543977_SKL_PDDG_Rev0_91



PEGATRON Title : CPU(6)_CPU GND

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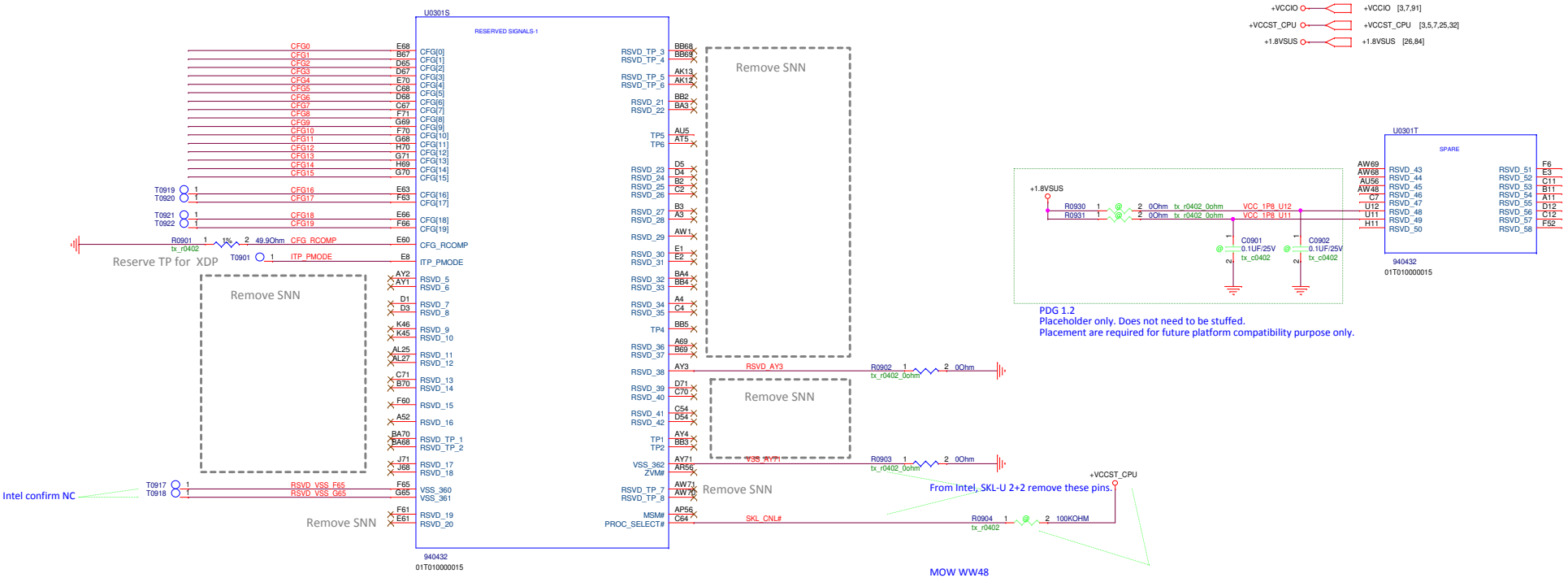
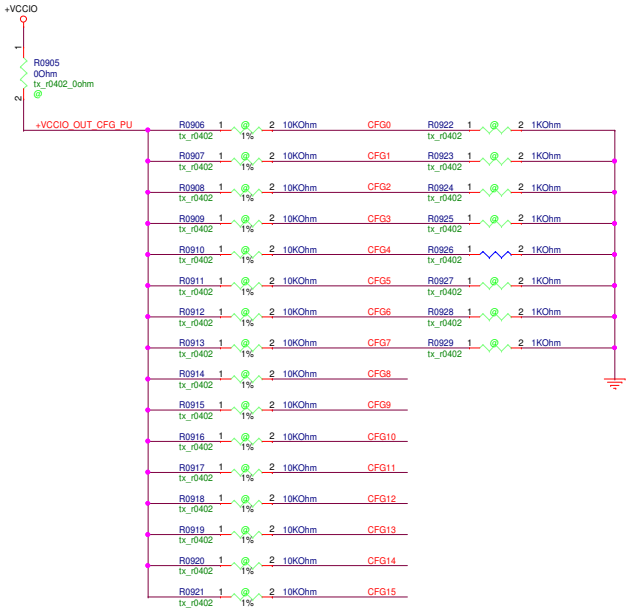
Engineer: Willy_Liao

Size	Project Name	Rev
C	HAWAII	0.0

Date: Thursday, March 31, 2016 Sheet 8 of 100



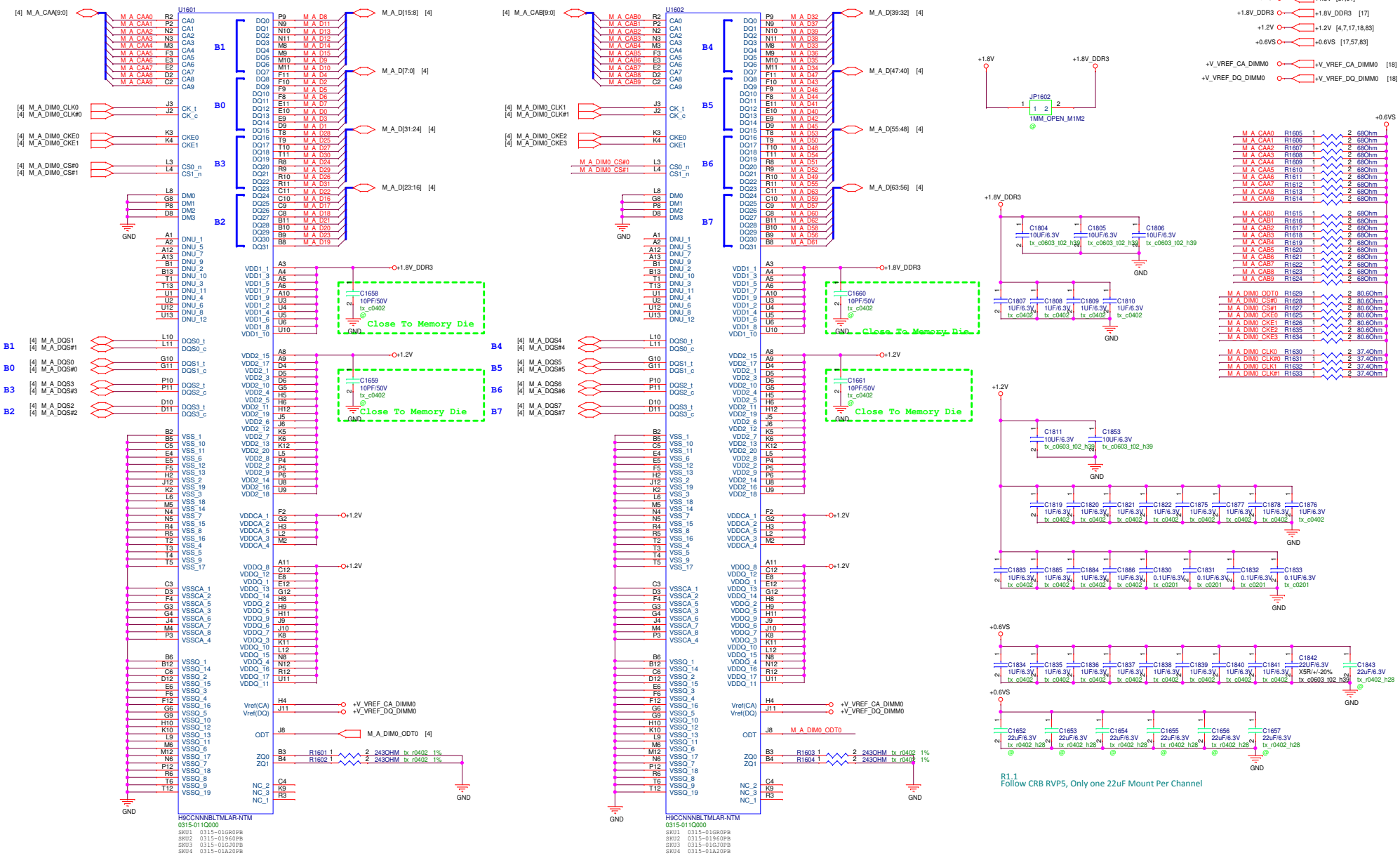


6.4 Reset and Miscellaneous Signals

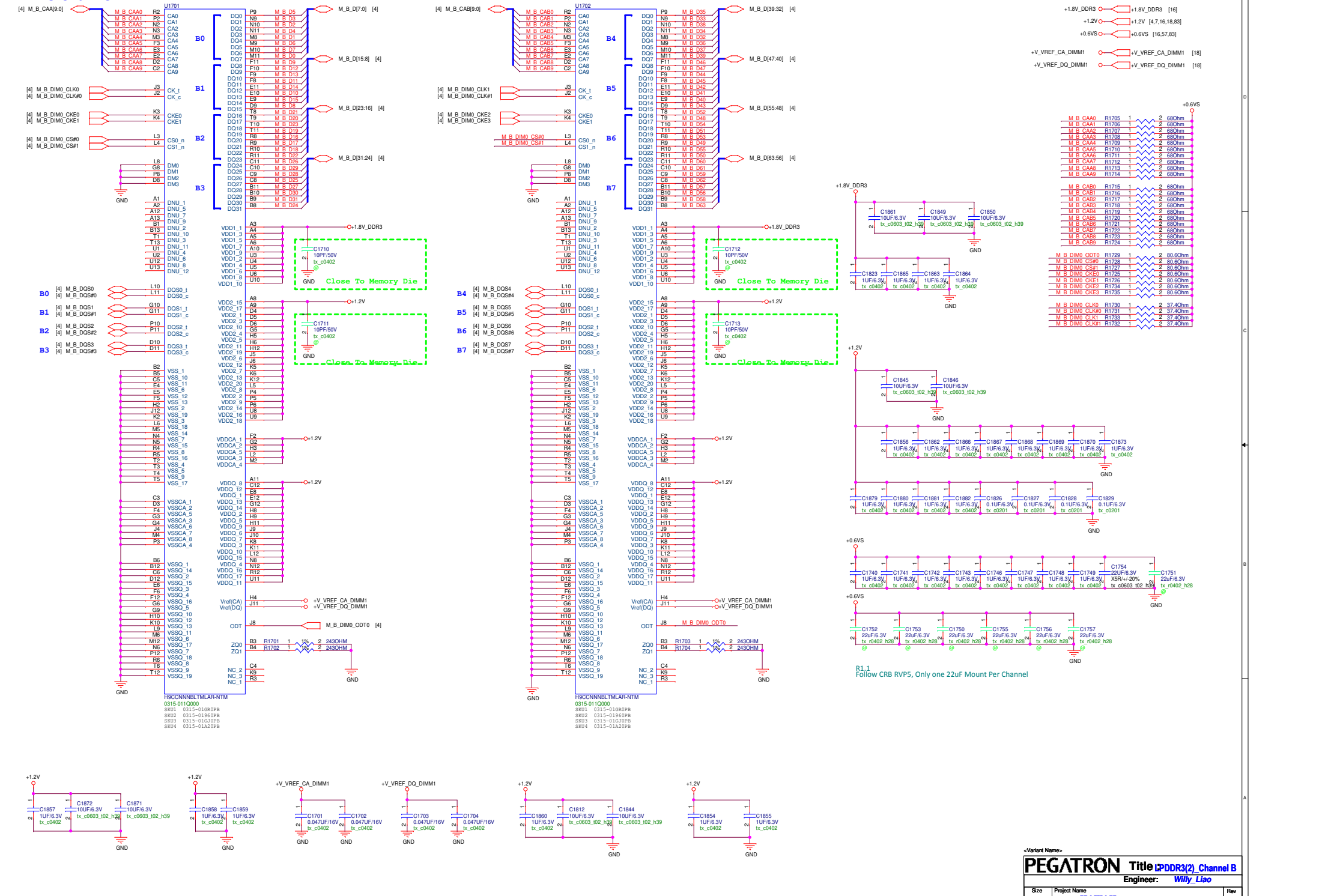
Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

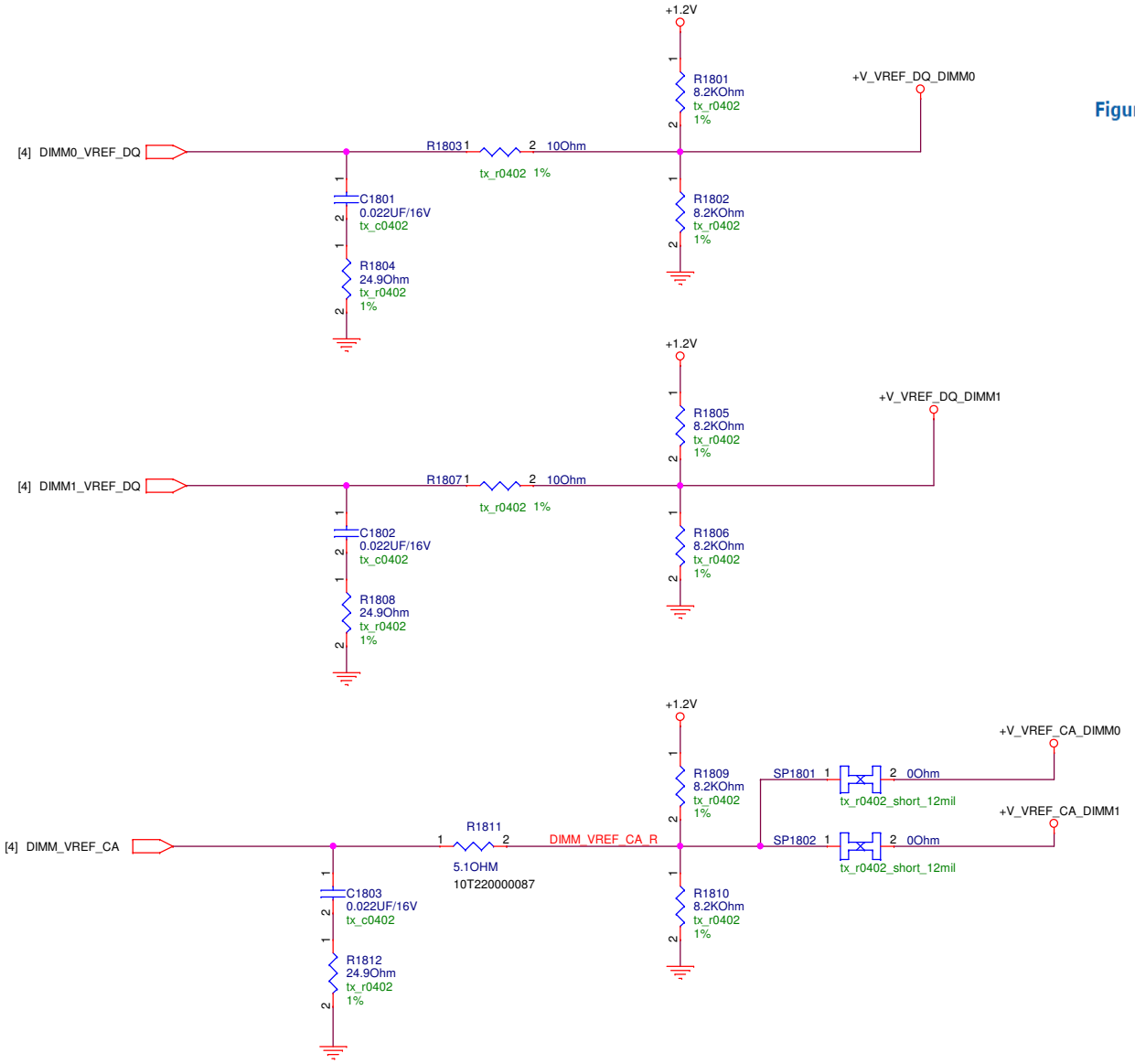
LPDDR3 Channel A



LPDDR3 Channel B



LPDDR3 Vref



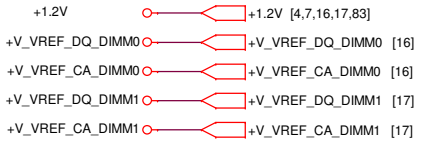
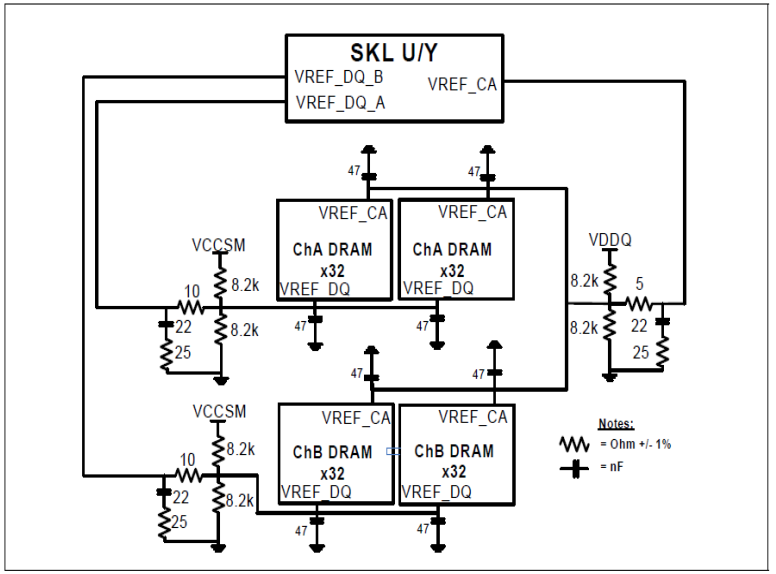
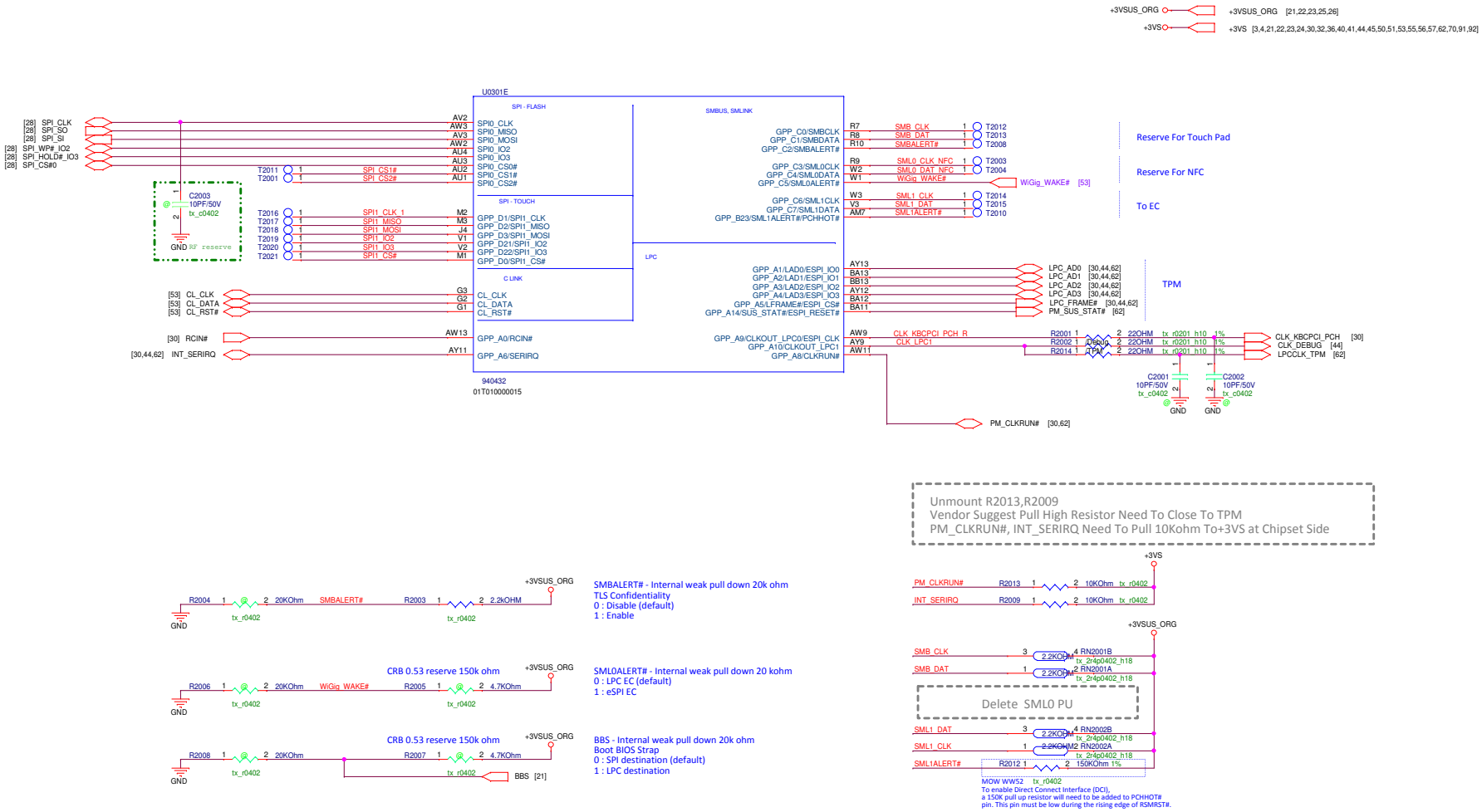


Figure 4-46. SKL U and SKL Y LPDDR3 x32 Memory Down V_{REF-DQ} and V_{REF-CA} Overview



PEGATRON	Title : LPDDR3(3)_CA/DQ	
BG1-NB4	Engineer: Willy_Liao	
Size: B	Project Name: HAWAII	Rev: 0.0
Date: Thursday, March 31, 2016	Sheet 18 of 100	

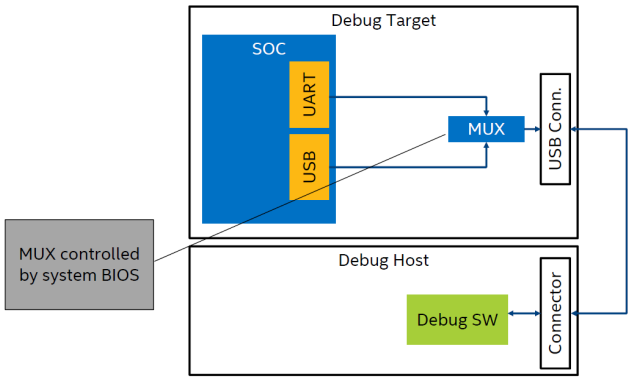


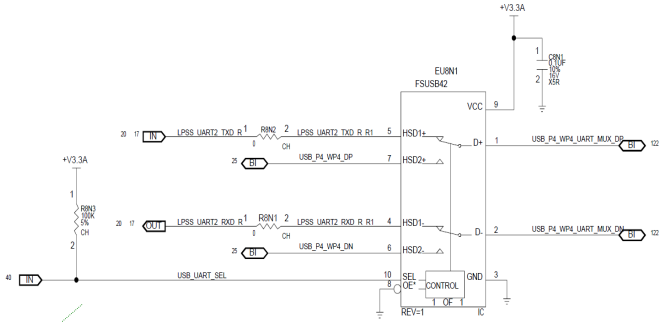
Unmount R2013,R2009
Vendor Suggest Pull High Resistor Need To Close To TPM
PM_CLKRUN#, INT_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

PEGATRON Title : PCH(1)_SPI/LPC
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: Willy_Liao
Size C | Project Name HAWAII | Rev 0.0
Date: Thursday, March 31, 2016 | Sheet 20 of 100

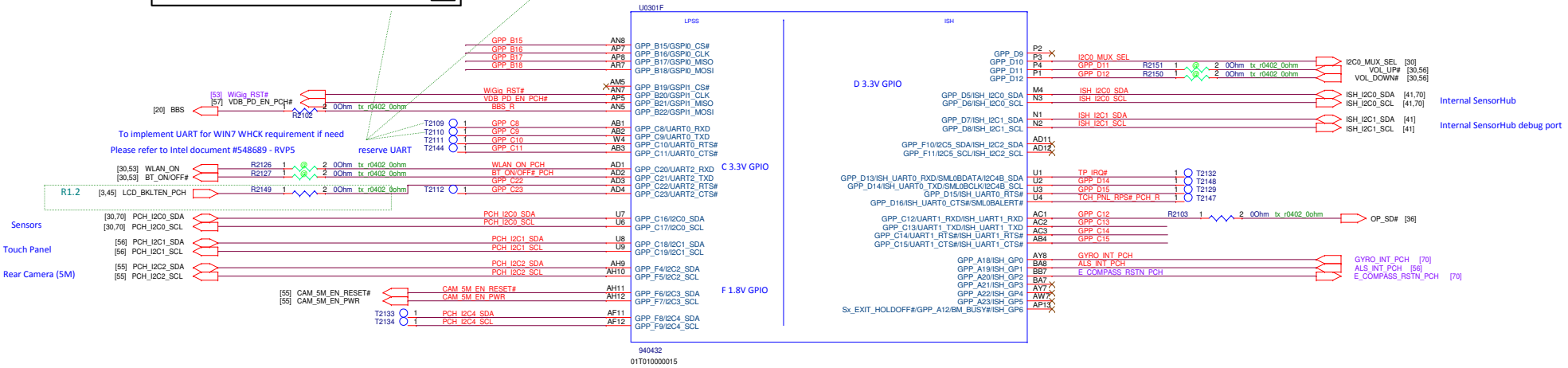
Microsoft* Windows* 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port.

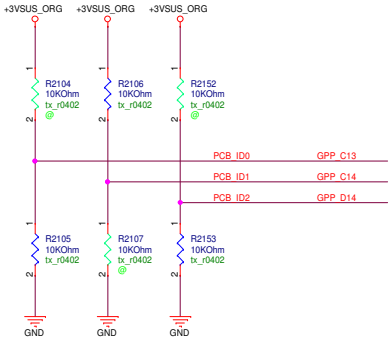
With skylake EHCI Removal, Potential Gap with Windows* 7 Kernel Debug and OS Installation – Mitigation Required





+3VS [3,4,20,22,23,24,30,32,36,40,41,44,45,50,51,53,55,56,57,62,70,91,92]

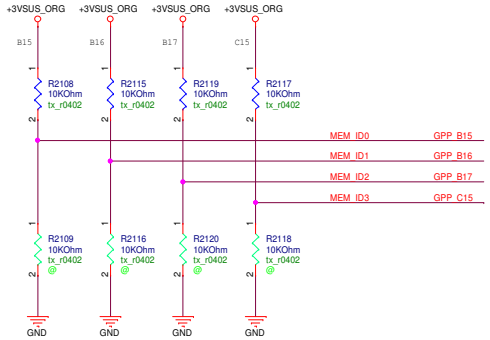




MB Version ID

	PCB_ID2 (GPP_D14)	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
A1 Build	1	0	0
A2 Build	1	0	1
B1 Build	1	1	0
B2 Build	1	1	1
C1 Build	0	0	0
C2 Build	0	0	1
PPR Build	0	1	0

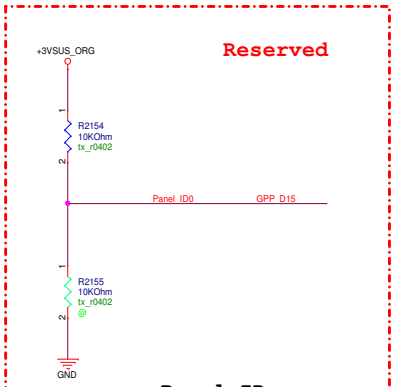
Hawaii (PPR build default)



Memory ID

A1	A2	B1	B2	EN	Vendor	Speed		GPP_C15	GPP_B17	GPP_B16	GPP_B15
SKU4		SKU2	SKU2	0315-01A20FB	SAMSUNG	1600	8G	0	0	0	1
	SKU1	SKU6	SKU6	0315-01960FB	SAMSUNG	1600	4G	0	0	1	0
					N/A	N/A	N/A	0	0	1	1
SKU1					HYNIX	1866	2G	0	1	0	0
SKU2					SAMSUNG	1600	2G	0	1	0	1
		SKU1	SKU1	0315-01GR0FB	HYNIX	1866	4G	0	1	1	0
		SKU3	SKU3	0315-01M90FB	SAMSUNG	1866	4G	0	1	1	1
		SKU5	SKU5	0315-01MT0FB	SAMSUNG	1866	8G	1	0	0	0

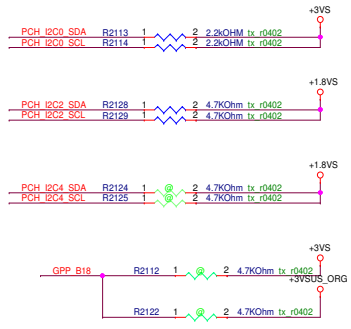
Hawaii (C build default)(SKU3)



Panel ID

Panel_ID0 (GPP_D15)	
AUO	1
PVO	0

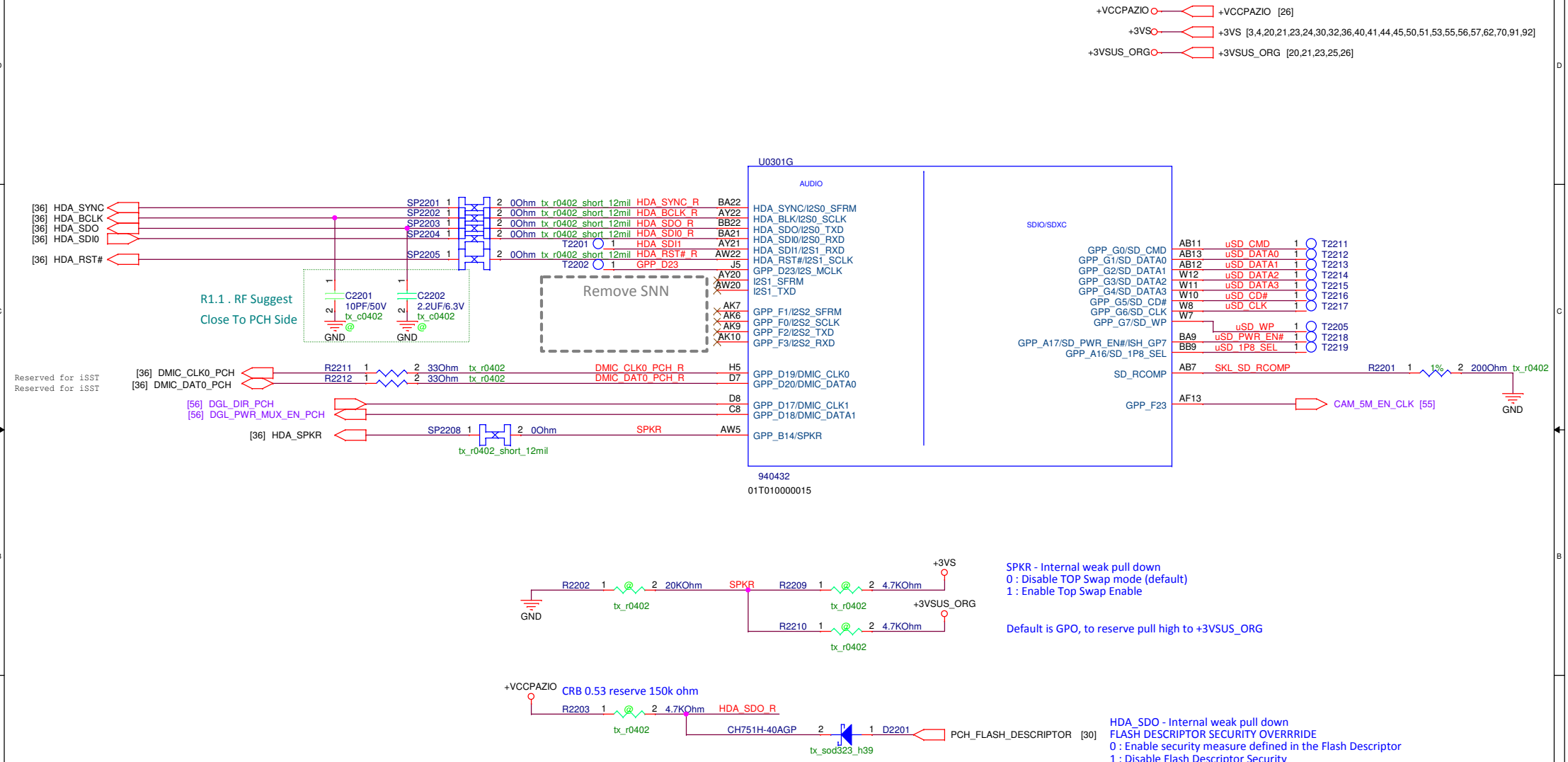
Hawaii (B2 build default)



GSPIO_MOSI / GPP_B18 - Internal weak pull down 20k ohm
0 : Disable No Reboot mode(default)
1 : Enable NO Reboot Enable mode

Default is GPO, to reserve pull high to +3VSUS_ORG

PEGATRON Title : PCH(2)_ISH
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: Willy_Liao
Size C | Project Name HAWAII | Rev 0.0
Date: Thursday, March 31, 2016 | Sheet 21 of 100



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCH(3)_HDA/SDIO

BG1-NB4

Engineer: Willy_Liao

Size	Project Name	Rev
B	HAWAII	0.0

Date: Thursday, March 31, 2016 Sheet 22 of 100

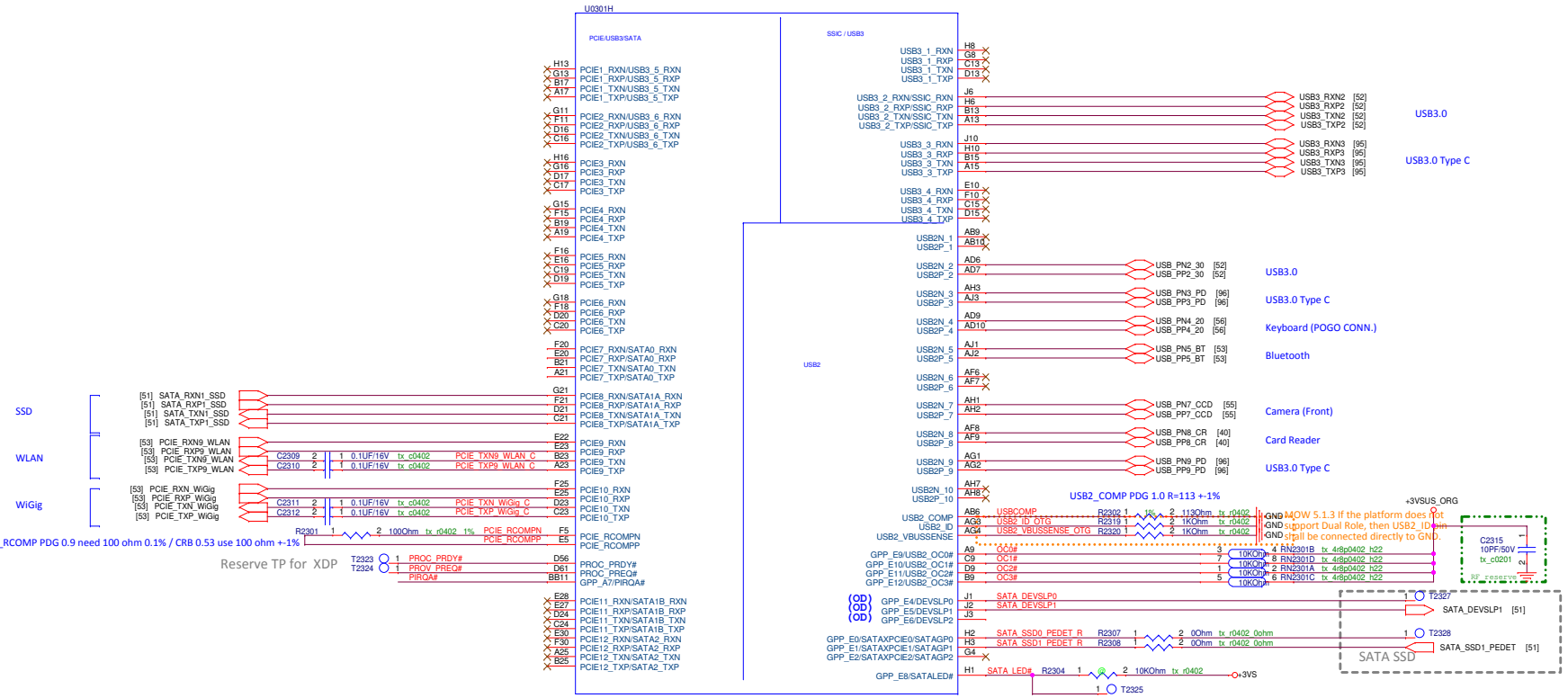


Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1_0_pub
Please refer the latest Doc.

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U

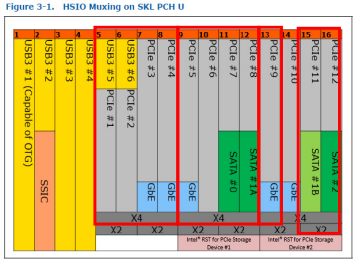
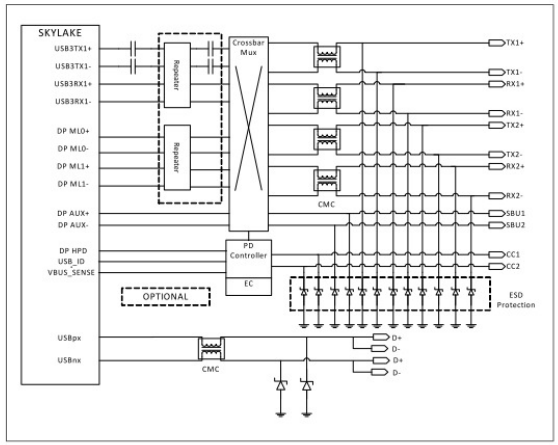
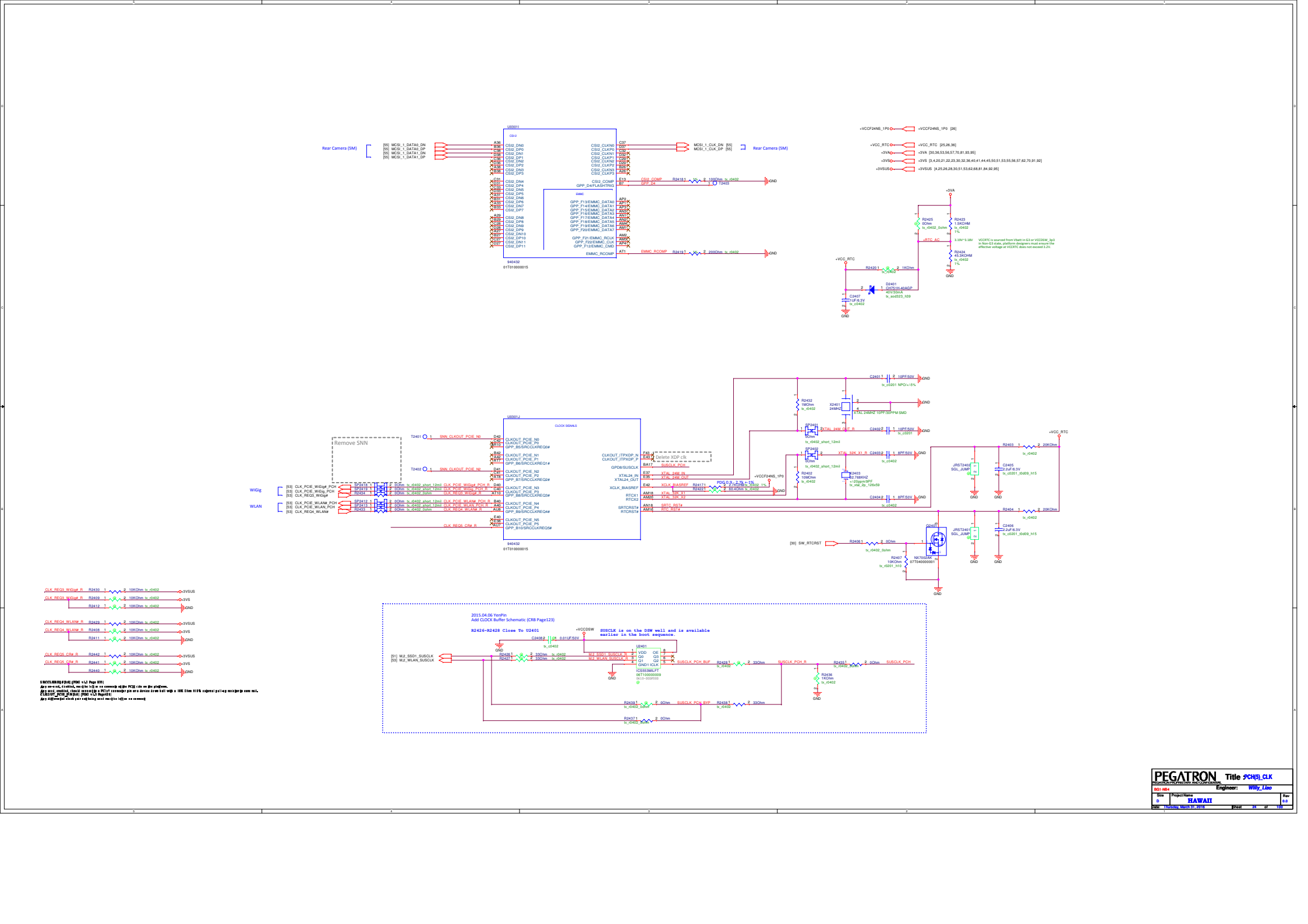


Figure 16-18.USB 3.0 Dual Role and DP x 2



Note: The figure above is a high level example implementation block; actual implementation on schematic may vary.

PEGATRON	Title:	PCH(4)_USB/PCIE/SATA	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-NB4	Engineer:	Willy_Liao	
Size: C	Project Name: HAWAII		Rev: 0.0
Date: Thursday, March 31, 2016	Sheet: 23	of: 100	



[55] MCSI_1_DATA0_DN
[55] MCSI_1_DATA0_DP
[55] MCSI_1_DATA1_DN
[55] MCSI_1_DATA1_DP

[SUSCLK_PCH_R (PCH)] (PCH 1.1 Page 870)
Always enabled, regardless of the assertion of any of the PCIe clock request signals.
[CLK_REQ5_CRd_R (PCH)] (PCH 1.1 Page 870)
Always asserted for Clock power management mechanism to remove

PEGATRON	Title: PCH(5)_CLK	
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer: Willy_Liao	
SG1-MB4		
Size: D	Project Name: HAWAII	Rev: 0.0
Date: Thursday, March 31, 2016	Sheet 24 of 100	

+3VSUS_ORG [20,21,22,23,26]
+VCC_RTC [24,26,36]
+VCCDSW [24,26,30]
+VCCST_CPU [3,5,7,9,32]
+3V [57,91]
+3VSUS [4,24,26,28,30,51,53,62,68,81,84,92,95]

+3VSUS_ORG
R2501 3KOhm tx_r0402 1%

U0301K
SYSTEM POWER MANAGEMENT

[30] PM_RSMRST# → SP2501 2 0Ohm tx_r0402_short_12mil → PLT_RST# / PM_SYS_RESET# / PM_RSMRST# → GPP_B13/PLTRST# / SYS_RESET# / RSMRST#
T2501 H_CPUPWRGD_TP → R2503 2 1KOhm tx_r0402 → H_CPUPWRGD → PROCPWRGD / VCCST_PWRGD
H_VCCST_PWRGD_MCP
ALL_SYS_PWRGD delay 99 ms from EC
[30,68] SYS_PWROK → R2504 2 0Ohm tx_r0402_0ohm → SYS_PWROK_R → SYS_PWROK / PCH_PWROK / DSW_PWROK
PM_PWROK → R2505 2 0Ohm tx_r0402_0ohm → PM_PCH_PWROK_R
PM_RSMRST_R → R2506 2 0Ohm tx_r0402_0ohm → PCH_DPWROK
[30] SUSWARN#/SUSPWRDNACK → R2508 2 0Ohm tx_r0402_0ohm → SUS_PWR_ACK_R → GPP_A13/SUSWARN#/SUSPWRDNACK / GPP_A15/SUSACK#
DSW function / non-AMT
[30] SUSACK# → R2509 2 0Ohm tx_r0402_0ohm → SUSACK# R
[53] WAKE_PCIE# → R2510 2 0Ohm tx_r0402_0ohm
T2502 GPD11 → LAN_WAKE# → WAKE#
T2508 GPD7 → GPD2/LAN_WAKE# / GPD11/LANPHYPC / GPD7/RSVD

940432
01T010000015

SLP_S0#:
When C10 use for
Low power mode

GPP_B12/SLP_S0# AT11 → SLP_S0# → SP2502 2 0Ohm tx_r0402_short_12mil → SLP_S0# [30] / PM_SUSB# [30,68] / PM_SUSC# [30,68]
GPD4/SLP_S3# AP15 → SLP_S3# R → SP2503 2 0Ohm tx_r0402_short_12mil
GPD5/SLP_S4# BA16 → SLP_S4# R
GPD10/SLP_S5# AY16 → GPD10 → T2504
SLP_SUS# AN15 → SLP_SUS# → T2510
SLP_LAN# AW15 → SLP_LAN# → T2505
GPD9/SLP_WLAN# BB17 → SLP_WLAN# → T2506
GPD6/SLP_A# AN16 → ME_PM_SLP_M# PCH → T2507
If Deep Sx is not implemented on the platform, this signal may be left as no connect
GPD3/PWRBTN# BA15
GPD1/ACPRESENT AY15 → AC_PRESENT_R → R2532 2 0Ohm tx_r0402_0ohm → PM_PWRBTN# [30] / ME_AC_PRESENT [30]
GPD0/BATLOW# AU13 → BATLOW#
+VCC_RTC
GPP_A11/PME#/INTRUDER# AU11 → PME# / AP16 → SM_INTRUDER# → R2513 2 1MOhm tx_r0402
GPP_B11/EXT_PWR_GATE# AM10 → MPHY_EXT_PWR_GATEB_R → T2509
GPP_B2/VRALERT# AM11 → VR_ALERT#
internal pull high

+3V
U2501 @ TC7SZ08FU 06T030000004
PLT_RST# → PLT_RST#_BUF [30,32,53,62]
C2502 100PF/50V tx_c0402 @
R2515 2 0Ohm tx_r0402_0ohm
C2503 100PF/50V tx_c0402 @
R2516 10KOhm tx_r0402
GND

[30,92] ALL_SYSTEM_PWRGD → SP2506 2 0Ohm tx_r0402_0ohm
[30] DELAY_ALL_SYSTEM_PWRGD → R2531 2 0Ohm tx_r0402_0ohm → ALL_SYSTEM_PWRGD_PMOK
[80,92] VRM_PWRGD → SP2507 2 0Ohm tx_r0402_short_12mil → VR_READY_PMOK
+3VSUS
U2502 TC7SH08FU
R2517 2 0Ohm tx_r0402_0ohm
PM_PWROK
R9229 10KOhm tx_r0402
GND

+VCCDSW
BATLOW# R2522 2 10KOhm tx_r0402
LAN_WAKE# R2523 2 10KOhm tx_r0402
GPD7 R2524 2 10KOhm tx_r0402
WAKE_PCIE# R2525 2 10KOhm tx_r0402
AC_PRESENT_R R2526 2 10KOhm tx_r0402
+3VSUS_ORG
PME# R2527 2 10KOhm tx_r0402
VR_ALERT# R2528 2 10KOhm tx_r0402
internal pull high
Set to GPI

EC delay ALL_SYSTEM_PWRGD 2ms
DELAY_ALL_SYSTEM_PWRGD R2529 2 0Ohm tx_r0402_0ohm
ALL_SYSTEM_PWRGD R2530 2 0Ohm tx_r0402_0ohm
H_VCCST_PWRGD_L → U2503 SN74AUP1G07DCKR 06T030000021
+3VSUS
C2504 0.1UF/16V tx_c0201
+VCCST_CPU
R9230 1KOhm tx_r0402
H_VCCST_PWRGD_R
R2521 2 60.4Ohm tx_r0402 1%
H_VCCST_PWRGD_MCP
C2505 0.1UF/16V tx_c0201 @
+VDDQ/+VCCST_CPU/+VCCSTG to VCCST_PWRGD must > 1ms

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: PCH(6)_POWER MANAGE
Engineer: Willy_Liao
BG1-NB4
Size: C
Project Name: HAWAII
Rev: 0.0
Date: Thursday, March 31, 2016
Sheet 25 of 100

Table 10-5. SKL U / SKL Y PCH-LP VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (A)	Details
0.064	All HSIO disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

SATA Gen3 Port X 10
PCIe Gen2 Lane X 1
USB3 Port X 2
All HSIO disabled (basic comsunption)
=0.154x1+0.132x1+0.132x4+0.064 = 1.01A

Decoupling cap for internal power

1.01A

Intel confirm pull down 1k

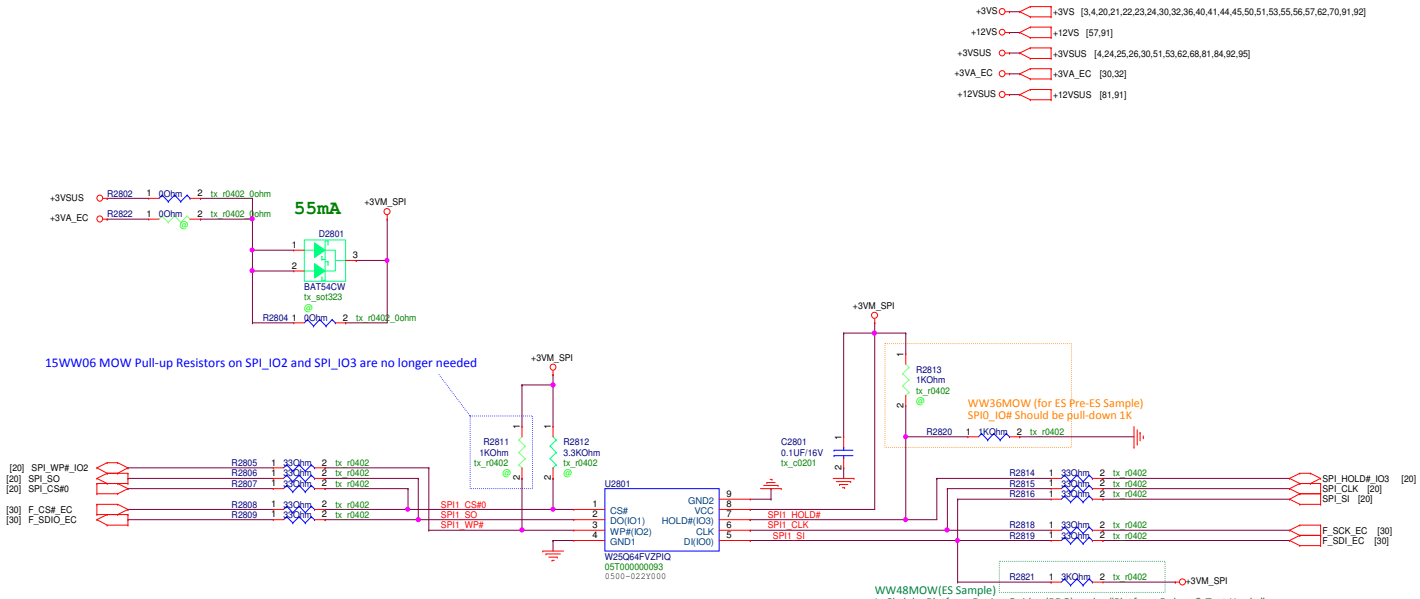
+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (tPCH06)

w/o DSW

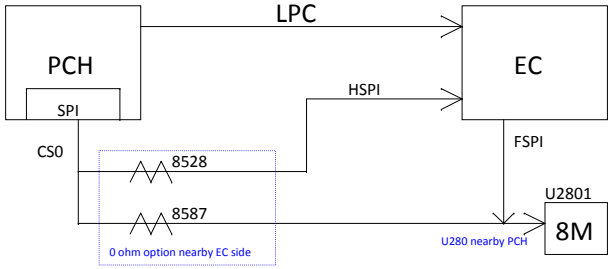
Remove +VCCMPHYGTAON_1P0_LS_P

if need choke, gate power should be disabled

Remove +VCCMPHYGTAON_1P0_LS_P



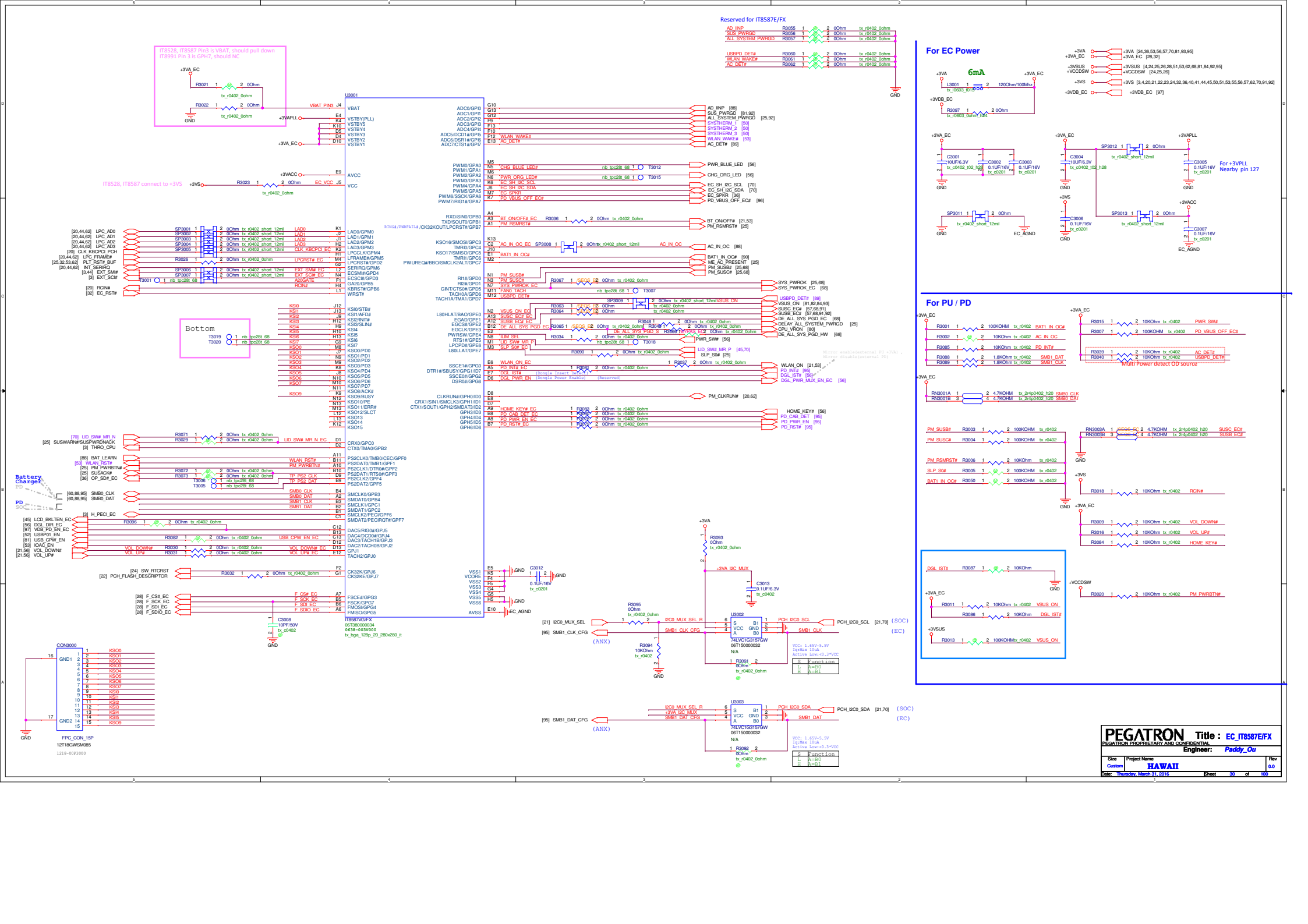
EC co-lay 8528/8587
SPI Structure

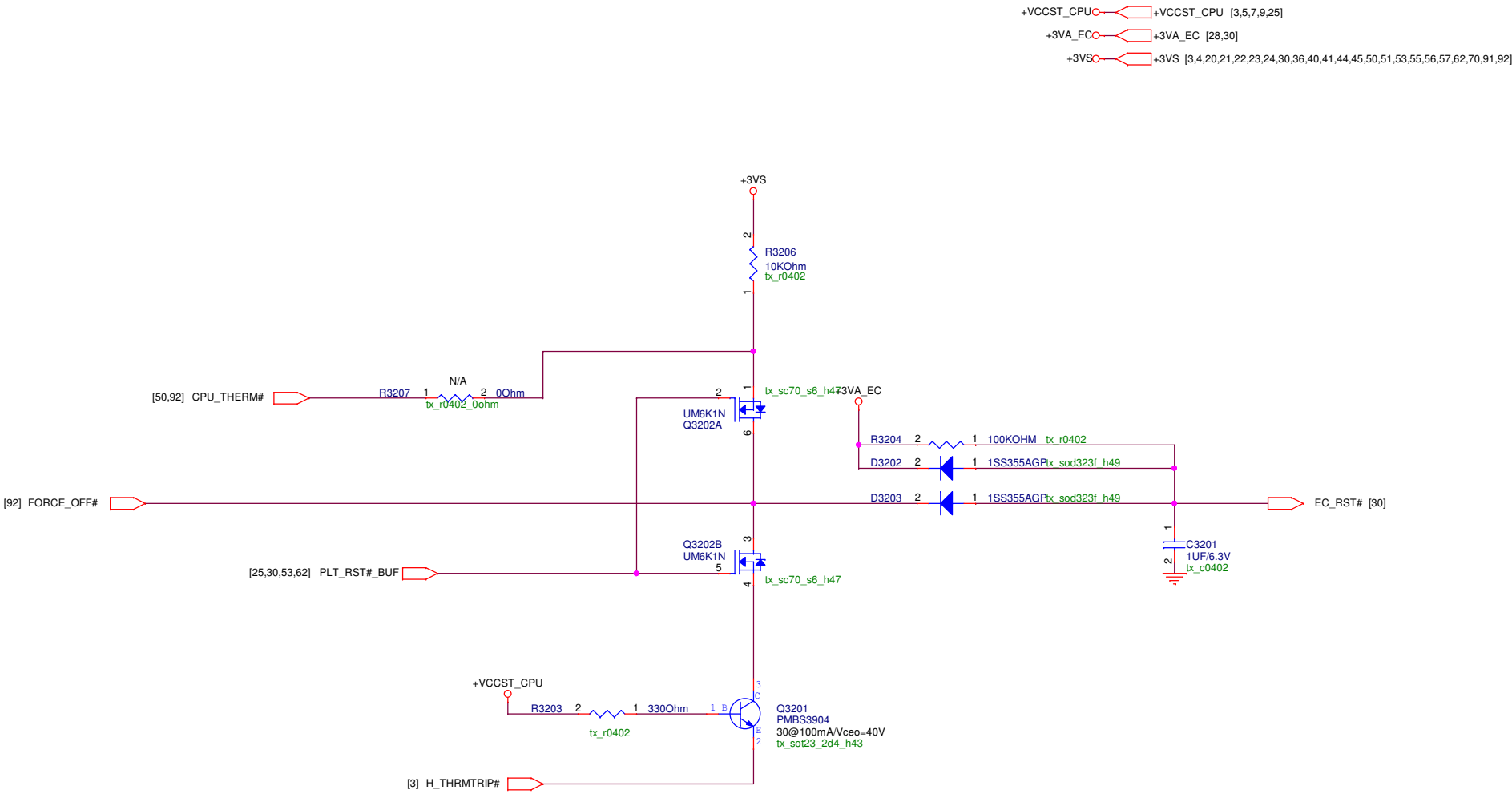


PCH SMBus

PCH

PEGATRON Title : PCH(9)_SPI,SMB
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: Willy_Liao
Size C | Project Name HAWAII | Rev 0.0
Date: Thursday, March 31, 2016 | Sheet 28 of 100


Reserved for IT8587E/FX
IT8528, IT8587 Pin3 is VBAT, should pull down
IT8991 Pin 3 is GPH7, should NC
IT8528, IT8587 connect to +3VS
Bottom
Battery Charger
PD
SOC
U3001
IT8587VG/FX
For EC Power
For PU / PD
6mA
For +3VPLL
Nearby pin 127
Multi Power detect OD source
CON3000
FPC_CON_15P
12T18GWSM085
PEGATRON
Title : EC_IT8587E/FX
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Paddy_Ou
Project Name HAWAII
Size Custom
Rev 0.0
Date: Thursday, March 31, 2016
Sheet 30 of 100



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RST_Reset Circuit

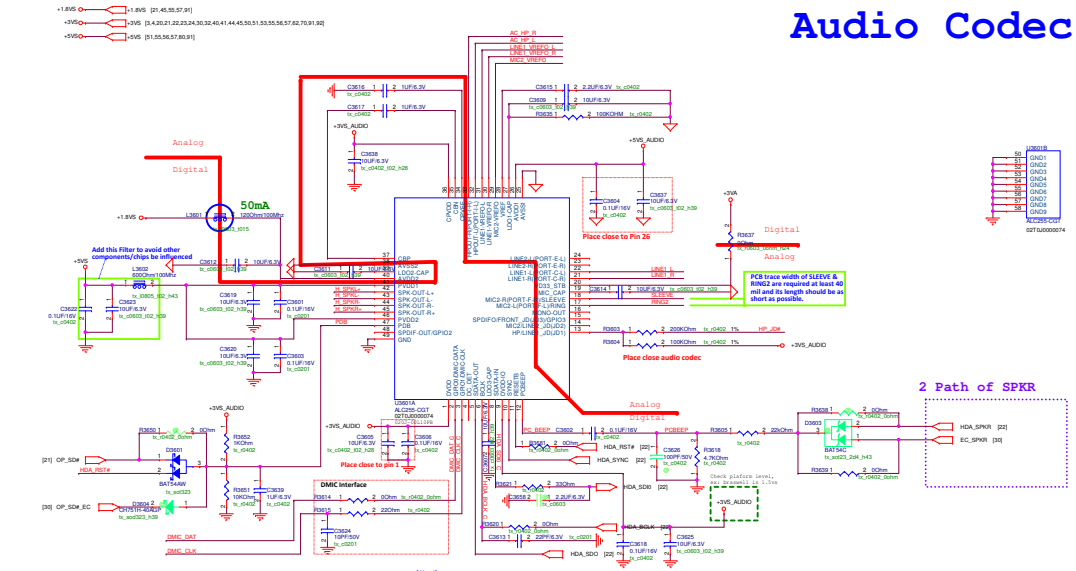
BG1-NB4

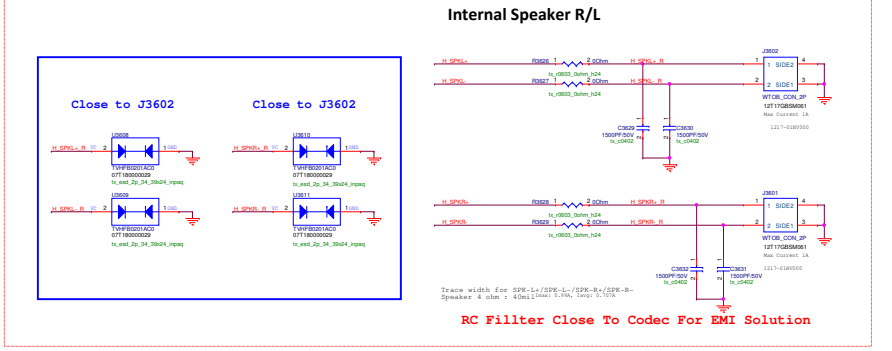
Engineer: Willy_Liao

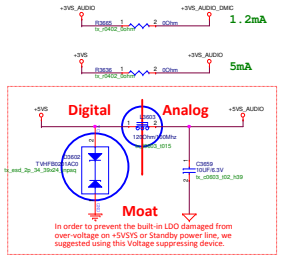
Size	Project Name	Rev
B	HAWAII	0.0

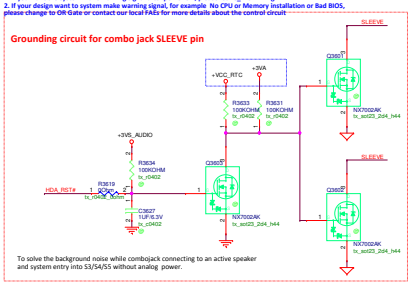
Date: Thursday, March 31, 2016 Sheet 32 of 100

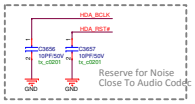
Audio Codec





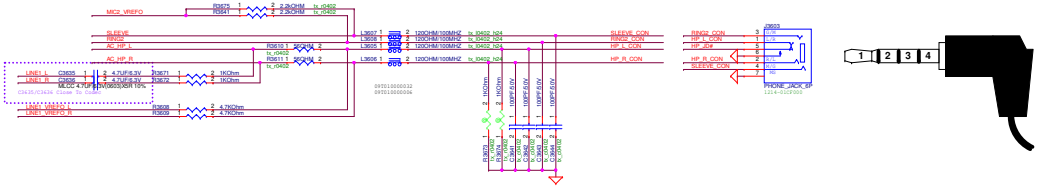


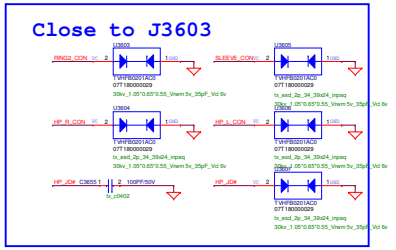




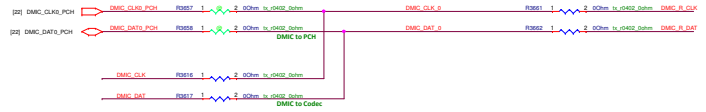
Universal Audio Jack

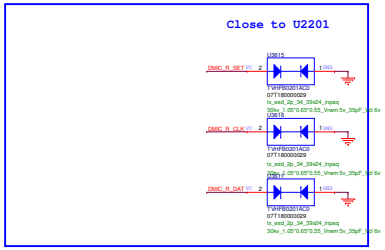
Supported iPhone/Nokia headset, Headphone, Line-In and Microphone through SW popup menu



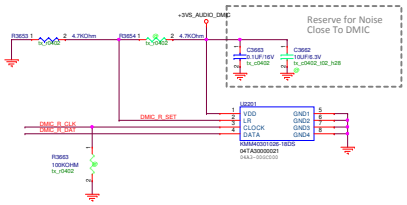


DMIC





DMIC_L



PEGATRON	Title :	AUD(1) ALC255	
MBRDC1WS	Engineer:	Willy_Liao	
Size: A1	Project Name: HAWAII		Rev: 0.6
Date: Thursday, March 31, 2016		Sheet 36 of 100	

Card Reader

+3VS +3VS [3,4,20,21,22,23,24,30,32,36,41,44,45,50,51,53,55,56,57,62,70,91,92]

Power Source

+3VS — 400mA — R4007 0Ohm tx_r0402_0ohm — +3VS_CR

RN4000A 10TK40000001 tx_2r4p1234_choke_4p_colay

[23] USB_PP8_CR — 0OHM — USB2_PP8_CR_R

L4000 90Ohm/100MHz 09T090000001 @

[23] USB_PN8_CR — 0OHM — USB2_PN8_CR_R

RN4000B tx_2r4p1234_choke_4p_colay

SD Power

+3VS_CARD_R

C4012 4.7uF/6.3V tx_c0402_t02_h26

C4013 0.1UF/16V tx_c0402

GND

Close to connector CON4001 Pin4

Close to U4001

T4001 1 XD_D7 V18

C4003 1UF/10V tx_c0603_t015 GND

SP14 SP13 SP12 SP11 — T4002 T4008

U4001A

R4005 6.2KOHM 1% tx_r0402

RREF_CR USB2_PN8_CR_R USB2_PP8_CR_R +3VS_CR +3VS_CARD SDREG

RREF DM DP 3V3_IN CARD_3V3 SDREG

SP10 GPIO0 SP9 SP8 SP7 SP6 — T4004 T4005 T4006

C4026 0.1UF/16V tx_c0402

C4004 1UF/10V tx_c0603_t015_h37

U4001B GND1 GND2 GND3 GND4 RTS5170_GR 02T0J0000041

RTS5170_GR 02T0J0000041

XD_CD# SP1 SP2 — T4009 T4003

SP5 SP4 SP3 — T4007

uSD Conn

+3VS_CARD — R4000 0Ohm tx_r0402_0ohm — +3VS_CARD_R

CON4001

SD_D1 SD_D0 SD_CLK_R SD_CMD SD_D3 SD_D2

13 12 GND2 DAT1 DAT0 VSS CLK VDD CMD DAT3/CD DAT2 GND1 11

COMMON CD

SD_CD#

SD_CARD_8P 12T21GBSM013 1221-00AS000

SD_CD# — R4006 0Ohm tx_r0402_0ohm @ — SD_WP

R4008 10KOhm tx_r0402

SD_CLK — R4002 0Ohm tx_r0402_0ohm — SD_CLK_R

C4011 2.2PF/50V tx_c0402 @

Close to U4001

+3VS_CR

C4005 10UF/10V tx_c0603_t02_h39

C4006 0.1UF/16V tx_c0402

ESD solution

Share Pin

SP1 SP3 SP4 SP6 SP10 SP12 SP13

SD_WP SD_D1 SD_D0 SD_CD# SD_CLK SD_CMD SD_D3 SD_D2

C4019 C4020 C4021 C4022 C4023 C4024 C4025 C4027 2.2PF/50V tx_c0402 @

+3VS_CARD_R

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

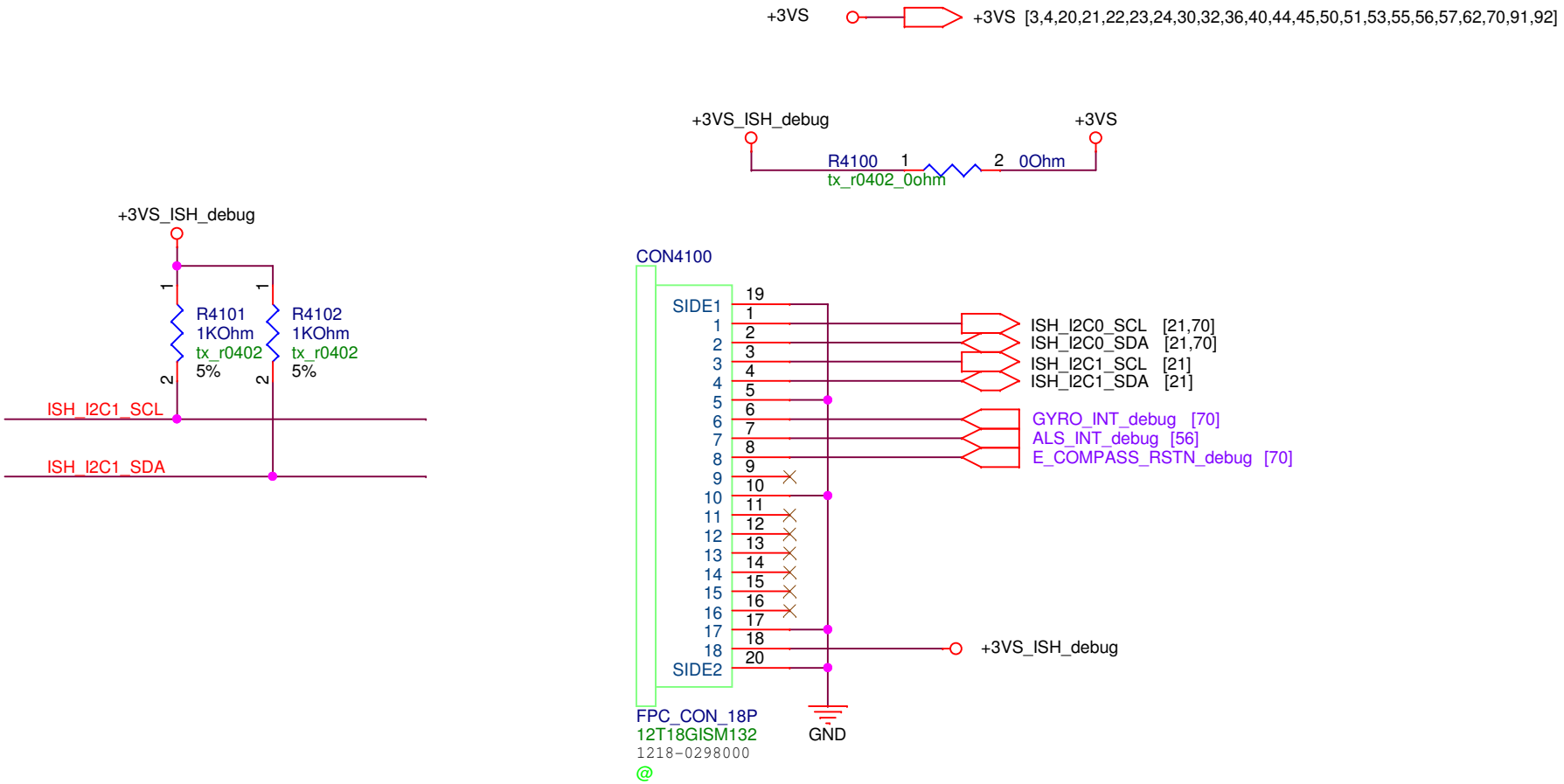
Title : Card Reader / uSD

Engineer: Willy_Liao

BG1/HW3

Size	Project Name	Rev
B	Hawaii	1.0

Date: Thursday, March 31, 2016 Sheet 40 of 100



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

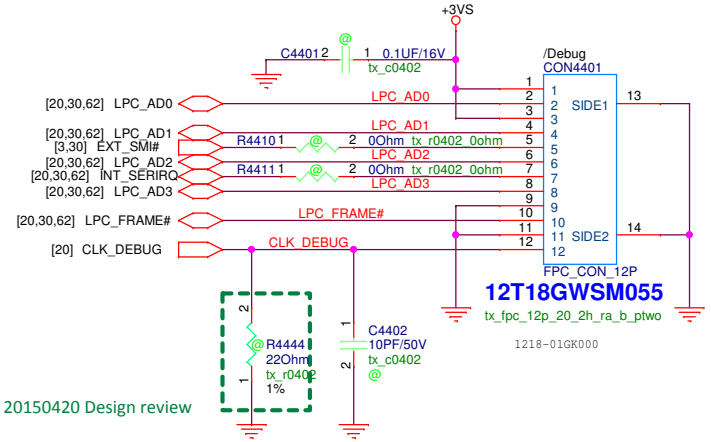
Title : ISH debug port

Engineer: *Willy_Liao*

Size	Project Name	Rev
A	**HAWAII**	0.0

Date: Thursday, March 31, 2016 Sheet 41 of 100

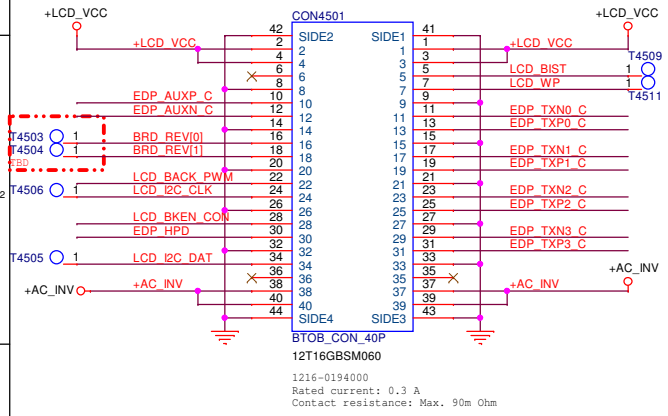
DEBUG CARD CONN.



141030 NO function Delete CON4402

PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : DEBUG CONN.	
BG1-NB4	Engineer: Willy_Liao	
Size: B	Project Name: HAWAII	Rev: 0.0
Date: Thursday, March 31, 2016	Sheet 44 of 100	

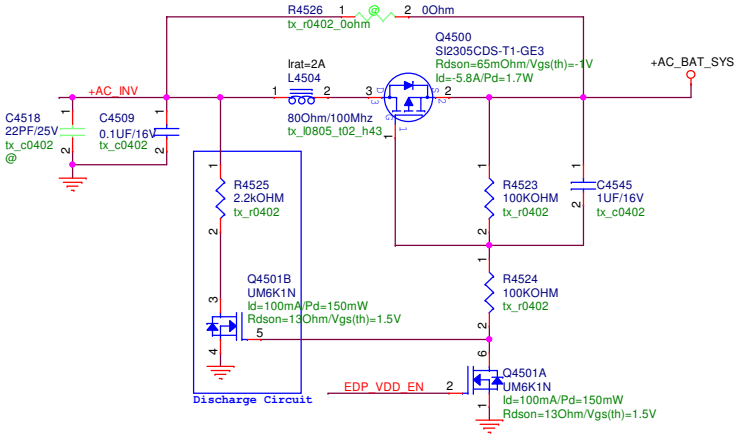
eDP



(LCD BL Power: 2.6W@7.5V=345mA)

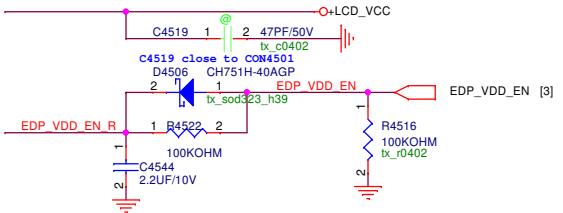
(LCD BL VLED 5.5V-7.5V-18V)

(7S6P)



(LCD Logic Power: 333mA)

(LCD VCC 3.0V-3.3V-3.6V)



(PL_PWM VIH:1.58V-1.8V, VIL:0V-0.47V)

(PL_PWM FREQ:200KHz-400KHz)

LCD_BACK_PWM TBD

(LCD Control Logic)

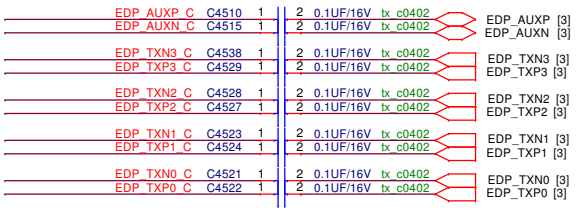
(BL_EN VIH:1.58V-4.3V, VIL:0V-0.47V)

LCD_BKEN_CON

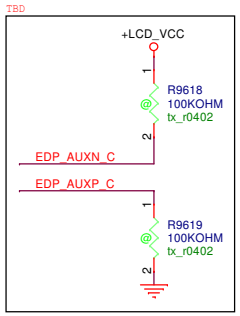
(HPD2 VOH:2.9V-3.3V-3.6V, VOL:0V-0.1V)

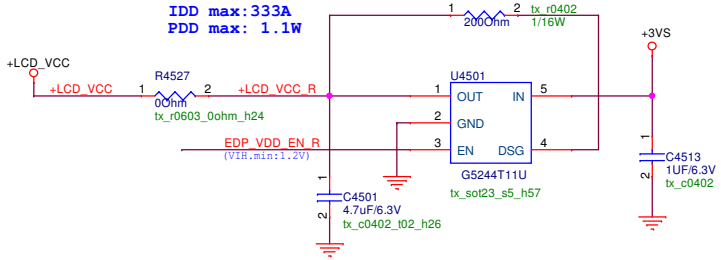
EDP_HPD [3]

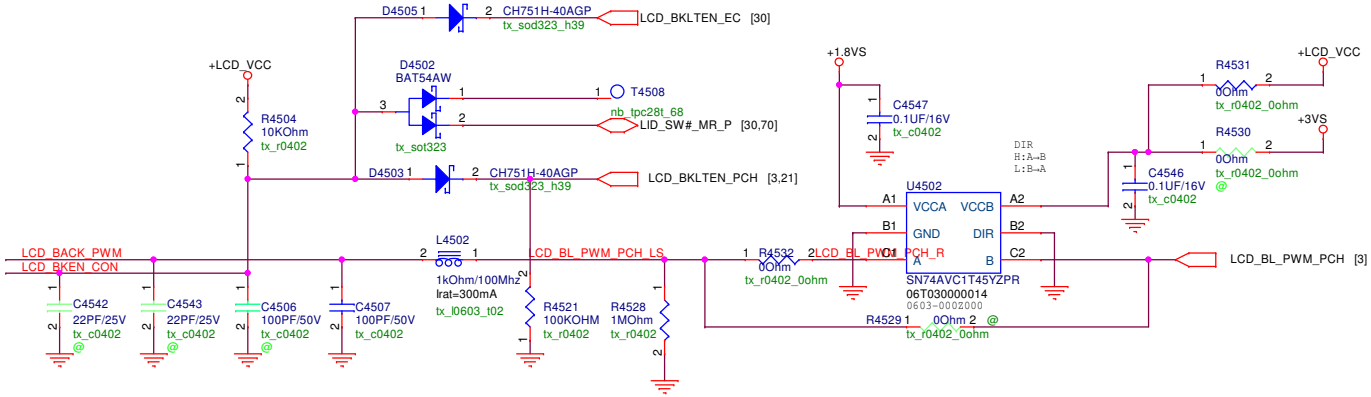
(LCD eDP 1.3 I/F)



LCD VDDEN / +LED_VCC







+1.8VS +1.8VS [21,36,55,57,91]

+3VS +3VS [3,4,20,21,22,23,24,30,32,36,40,41,44,50,51,53,55,56,57,62,70,91,92]

+5VS +5VS [36,51,55,56,57,80,91]

+AC_BAT_SYS +AC_BAT_SYS [80,81,82,83,88,97]

PEGATRON Title : LCM_EDP

Engineer: Paddy_Ou

Size	Project Name	Rev
A3	HAWAII	0.0

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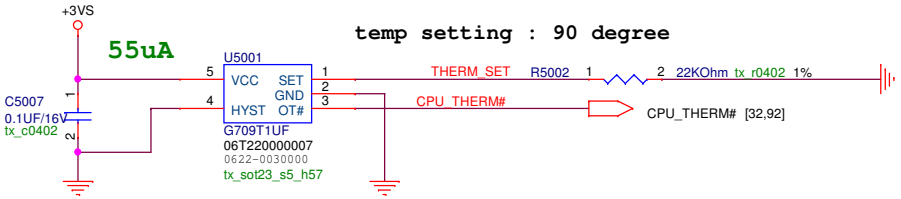
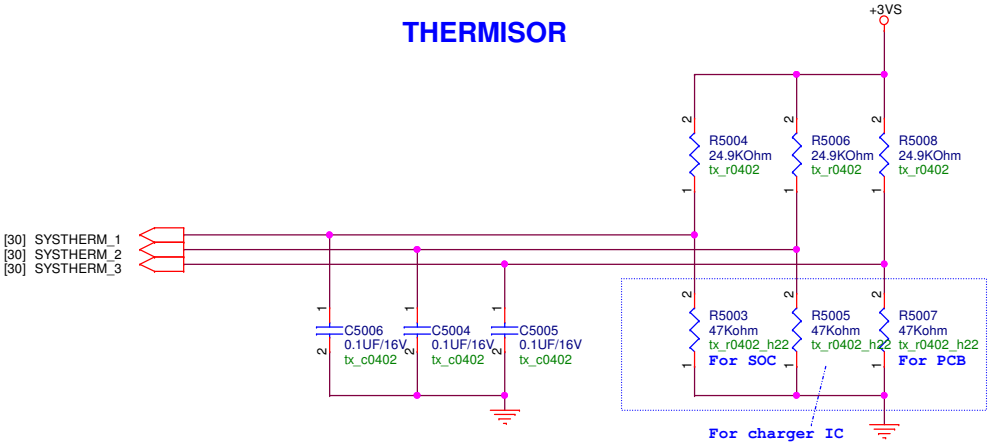
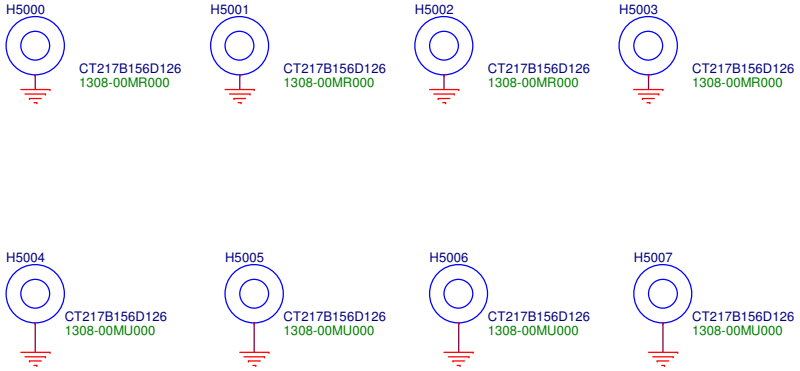
G709 Thermal Sensor



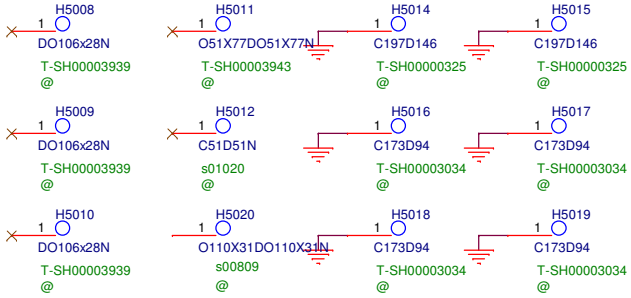
THERMISOR



Nut (for CPU)



Screw Hole / Tooling Hole (for hawaii_main_pcb_layout_0930)



PEGATRON Title : Thermal/Fan

BG1-NB4 Engineer: Paddy_Ou

Size	Project Name	Rev
B	HAWAII	0.0

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NGFF socket B -- Main SSD

PCIe_M.2_Electromechanical_Spec_Rev_0.9-3_07312013_RS_Clean

Table 46. Socket 2 Module Configuration Table

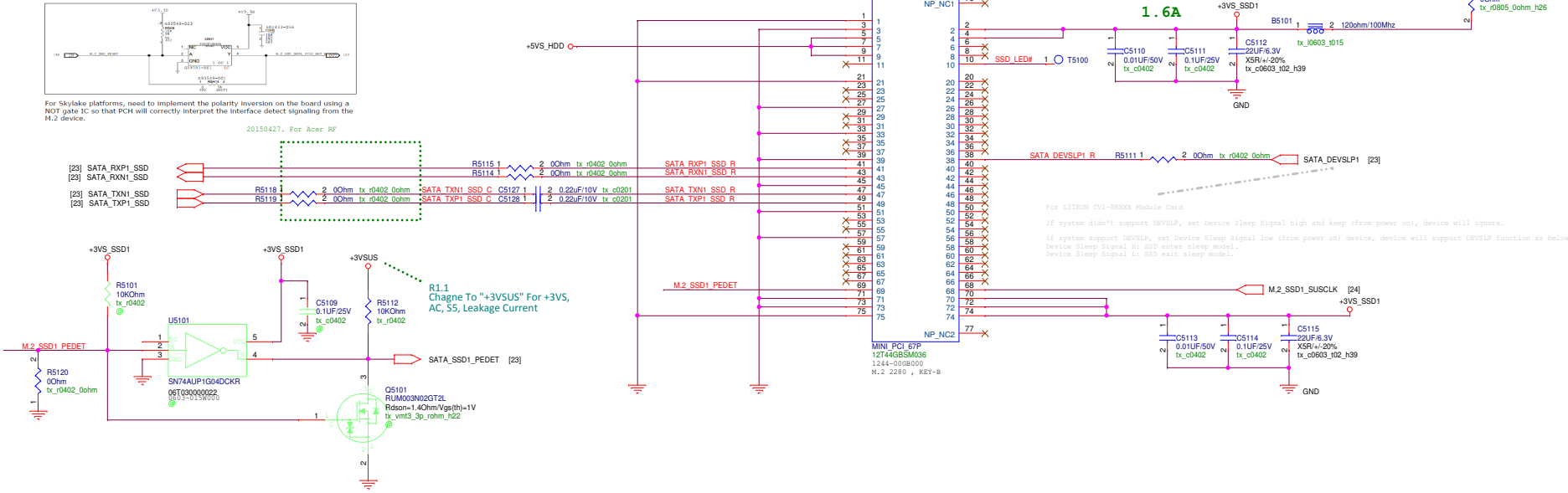
Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A

36.3.2.3 PEDET Guidelines

PEDET is the interface detect used by PCH to determine the communication protocol that the M.2 card uses; PCIe* signaling (high) or SATA signaling (low) in conjunction with a platform located pull-up resistor.

Figure 36-6. PEDET Circuitry Example

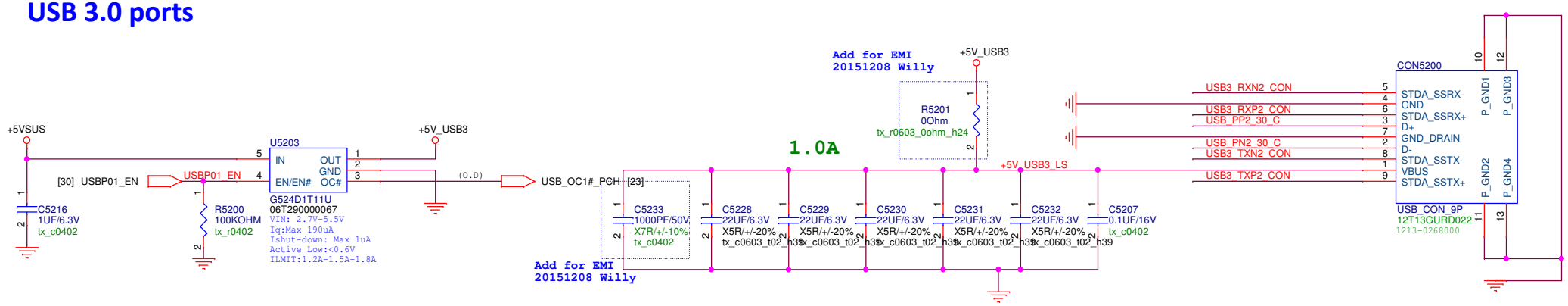
For Skylake platforms, need to implement the polarity inversion on the board using a NOT gate IC so that PCH will correctly interpret the interface detect signaling from the M.2 device.

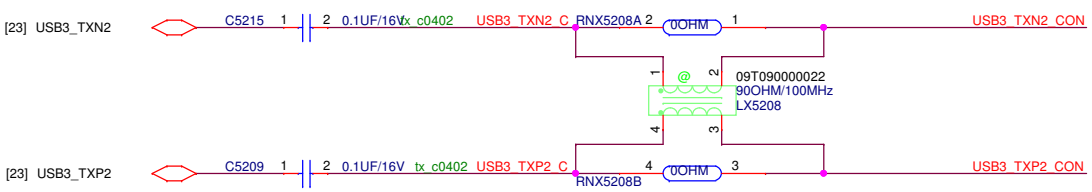


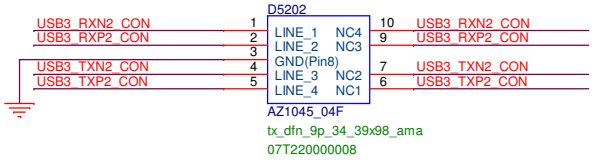
PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON	Title : NGFF SSD	
BG1-NB4	Engineer: Willy_Liao	
Size: C	Project Name: HAWAII	Rev: 0.0
Date: Thursday, March 31, 2016	Sheet 51 of 100	

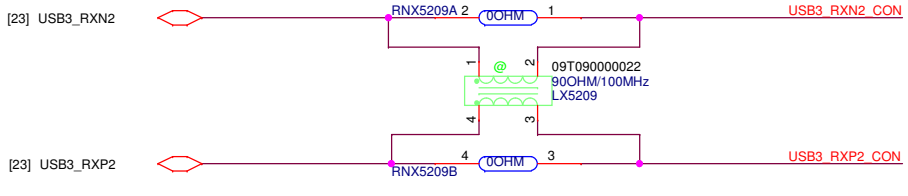
USB 3.0 ports

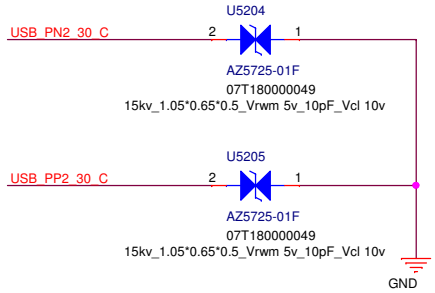


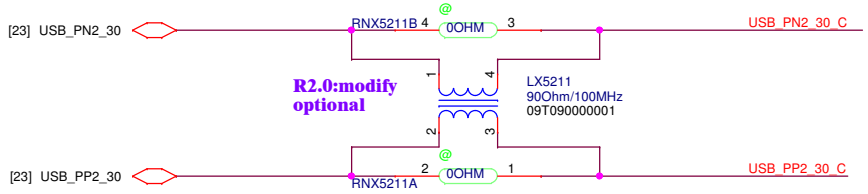


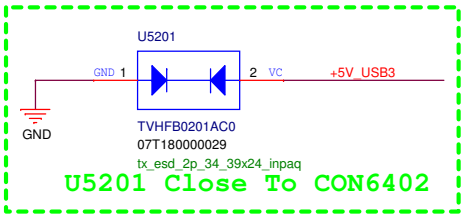


PLACE ESD Diodes near USB Connector









PEGATRON Title : USB3.0

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Willy_Liao

Size	Project Name	Rev
B	HAWAII	0.0

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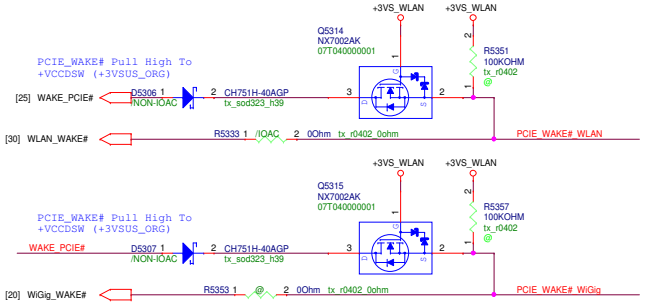
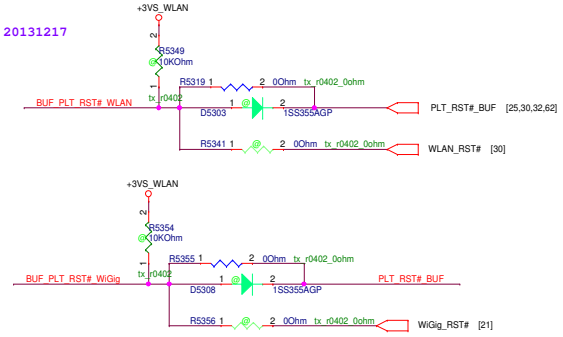
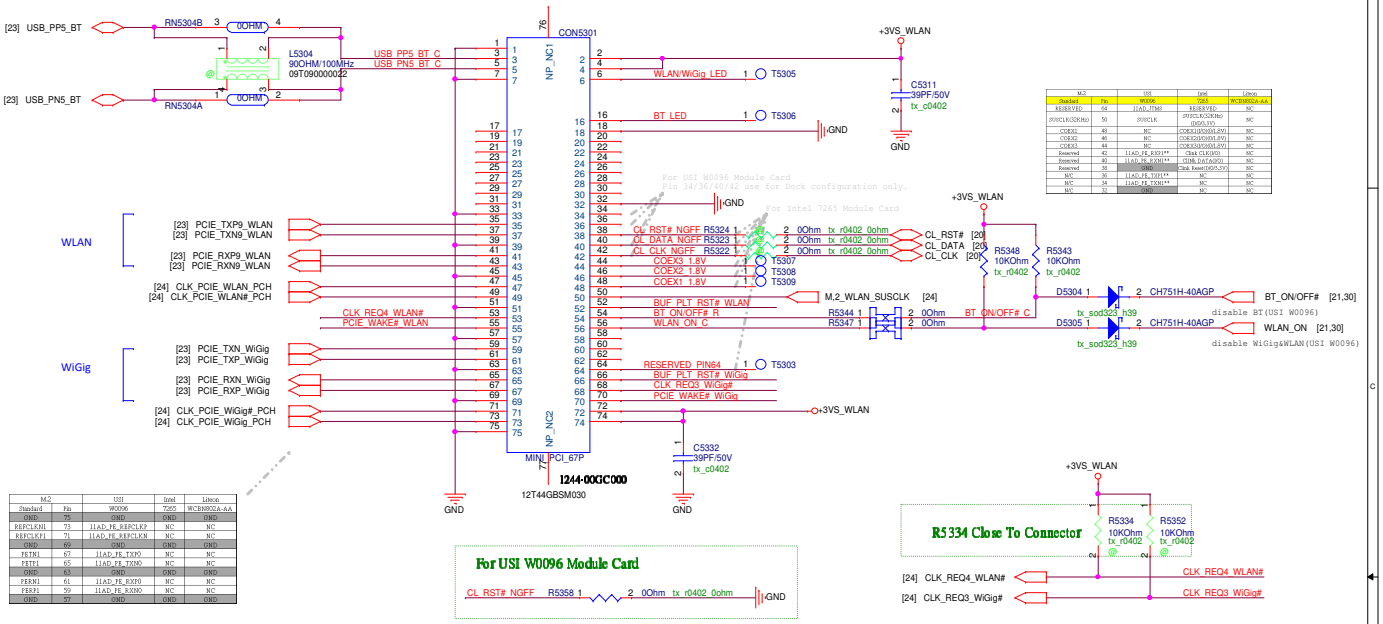
WLAN / WiGig / BT with NGFF socket E
For USI W0096 Module Card





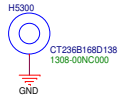


M.2 Standard	Pin	USI W0096	Intel 7265	Lite-on WCBN802A-AA
GND	75	GND	GND	GND
REFCLKM1	73	11AD_PE_REFCLKP	NC	NC
REFCLKP1	71	11AD_PE_REFCLKN	NC	NC
GND	69	GND	GND	GND
PETN1	67	11AD_PE_TXP0	NC	NC
PETP1	65	11AD_PE_TXN0	NC	NC
GND	63	GND	GND	GND
PERN1	61	11AD_PE_RXP0	NC	NC
PERP1	59	11AD_PE_RXN0	NC	NC
GND	57	GND	GND	GND

M.2 Standard	Pin	USI W0096	Intel 7265	Lite-on WCBN802A-AA
RESERVED	64	11AD_TIM0	RESERVED	NC
SUSCLK(32KHz)	50	SUSCLK	SUSCLK(32KHz) (DEVSLP)	NC
COEX1	48	NC	COEX1(V2G0.18V)	NC
COEX2	46	NC	COEX2(V2G0.18V)	NC
COEX3	44	NC	COEX3(V2G0.18V)	NC
Reserved	42	11AD_PE_RST0**	Clink CLK(0V)	NC
Reserved	40	11AD_PE_WAKE0**	CLINK DATA(0V)	NC
Reserved	38	GND	Clink Reset(DEVSLP)	NC
NC	36	11AD_PE_TX1**	NC	NC
NC	34	11AD_PE_TX0**	NC	NC
NC	32	GND	NC	NC

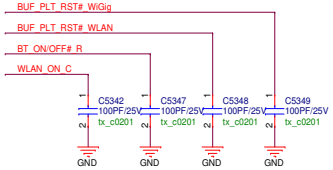
Antenna Cable Cilp

Nut(for WIFI card)

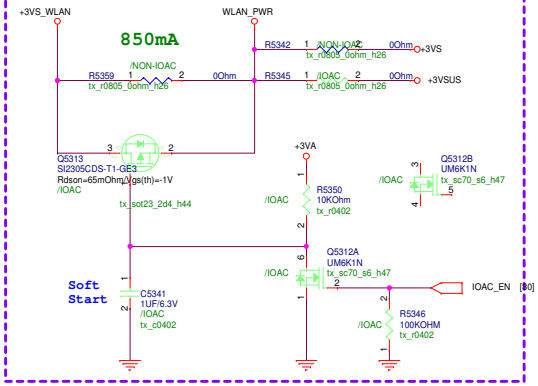


P/N:1308-00NC000

EMI Solution



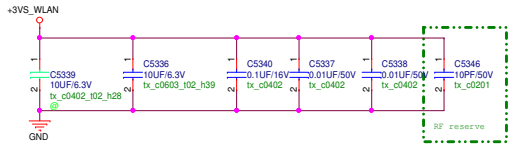
IOAC Control Schematic



+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 2,4

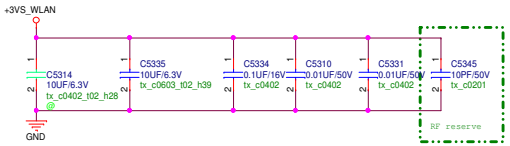
Place 10UF near +3V_WLAN_WP1 source side.



+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : NGFF WLAN / WiGig

Engineer: Willy_Liao

Size	Project Name	Rev
C	HAWAII	0.0

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CO-LAY

2M Camera (Front)

Power Source(ISP)

ESD solution

close to CON5501

close to CON5502

close to Chip

For PIN 1

For PIN 29

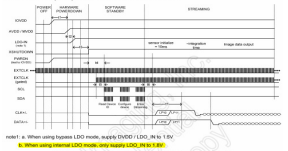
Camera Power(2M)

close to CON5501

reserve

Power Sequence (HM2051)

9.4.1. Power-up Sequence with Hardware Shutdown



note1 : a. When using bypass LDO mode, supply DVDD / LDO_IN to 1.8V

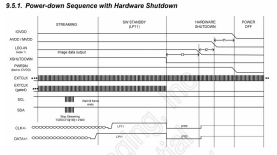
b. When using internal LDO mode, only supply LDO_IN to 1.8V

Figure 29: Power-up Sequence with Hardware Shutdown (XSHUTDOWN)

Symbol	Parameter	Min	Max	Unit
t1	IOVDD to AVDD/MVDD	0	∞	sec.
t2	AVDD/MVDD to LDO_IN	0	∞	sec.
t3	LDO_IN to XSHUTDOWN	0	∞	sec.
t4	XSHUTDOWN to SDA / SCL transaction	100 us		MCLK
t5	XSHUTDOWN (Gated Clock) to SDA / SCL	100 us		MCLK
t6	PLL Lock Time	100 us		sec.
t7	Enter Streaming Time (fixed)	1.3 ms		sec

Table 8: Power-up sequence timing (XSHUTDOWN)

9.5.1. Power-down Sequence with Hardware Shutdown



note1 : a. When using bypass LDO mode, supply DVDD / LDO_IN to 1.5V

b. When using internal LDO mode, only supply LDO_IN to 1.8V

Figure 30: Power-down without UPLS Sequence (XSHUTDOWN)

Symbol	Parameter	Min	Max	Unit
t1	AVDD/MVDD to IOVDD	0	∞	sec.
t2	LDO_IN to AVDD/MVDD	0	∞	sec.
t3	XSHUTDOWN to LDO_IN	0	∞	sec.

Table 9: Power-down without UPLS sequence timing (XSHUTDOWN)

Canmera Power (5M)

close to CON5502

5M Camera (Rear)

CO-LAY

Power Sequence (OV5670)

figure 2-3 power up sequence (case 1)

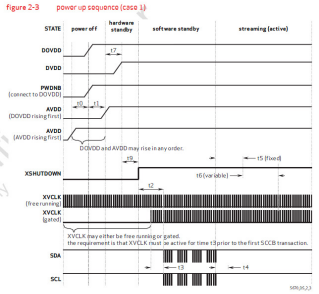


table 2-4 power up sequence timing constraints (sheet 1 of 2)

constraint	label	min	max	unit
AVDD rising – DOVDD rising	t0	0	∞	ns
DOVDD rising – AVDD rising	t1			ns
XSHUTDOWN rising – first SCCB transaction	t2	8192		XVCLK cycles
minimum number of XVCLK cycles prior to the first SCCB transaction	t3	8192		XVCLK cycles
PLL start up/lock time	t4		0.2	ms
entering streaming mode – first frame start sequence (fixed part)	t5		10	ms

table 2-4 power up sequence timing constraints (sheet 2 of 2)

constraint	label	min	max	unit
entering streaming mode – first frame start sequence (variable part)	t6	delay is the exposure time value		lines
AVDD or DOVDD, whichever is last – DVDD	t7	0	∞	ns
DVDD – PWDNB rising	t8	0	∞	ns
DVDD – XSHUTDOWN rising	t9	0	∞	ns

figure 2-6 power down sequence (case 1)

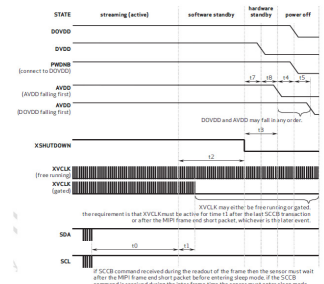


table 2-6 power down sequence timing constraints

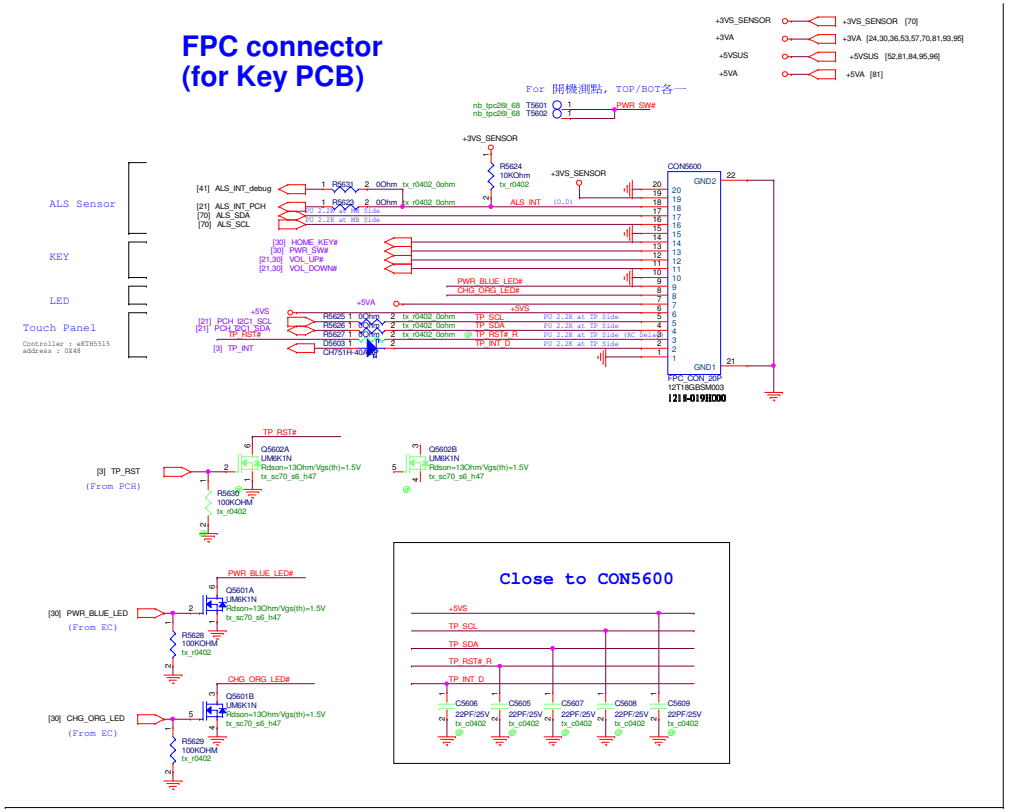
constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0		when a frame of MIPI data is output, wait for the MIPI end code before entering the software for standby; otherwise, enter the software standby mode immediately	
minimum of XVCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		XVCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDOWN falling	t2	512		XVCLK cycles
XSHUTDOWN falling – AVDD falling or DOVDD falling whichever is first	t3	0.0		ns
AVDD falling – DOVDD falling	t4	AVDD and DOVDD may fall in any order, the falling separation can vary from 0 ns to infinity		ns
DOVDD falling – AVDD falling	t5			ns
PWDNB falling – DOVDD falling	t6	0.0		ns
XSHUTDOWN falling – DVDD falling	t7	0.0		ns
DVDD falling – AVDD falling or DOVDD falling whichever is first	t8	0.0		ns
PWDNB falling – DVDD falling	t9	0.0		ns

PEGATRON Title : Camera 2M/5M

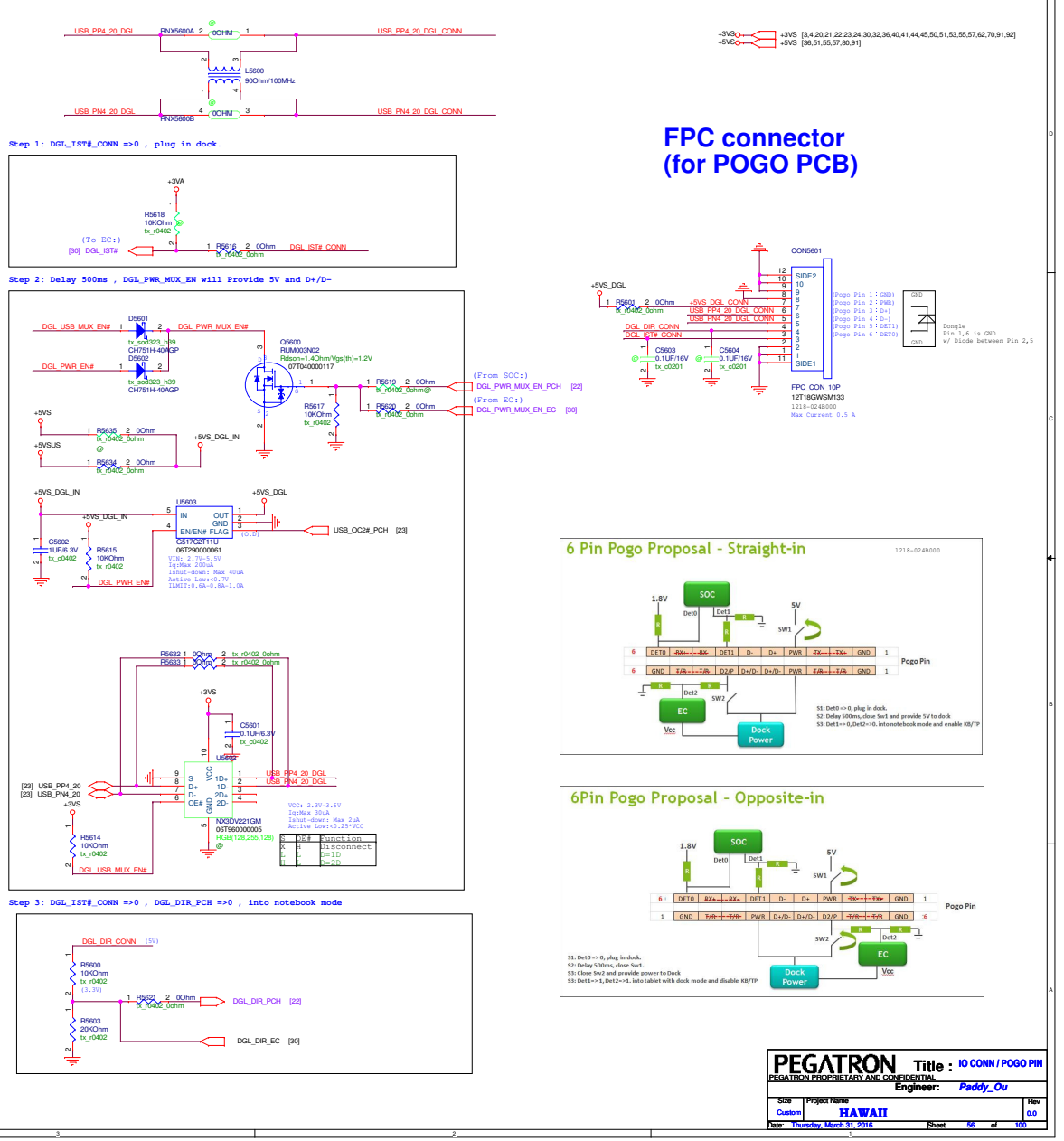
Engineer: Willy_Liao

HAWAII

FPC connector (for Key PCB)



FPC connector (for POGO PCB)

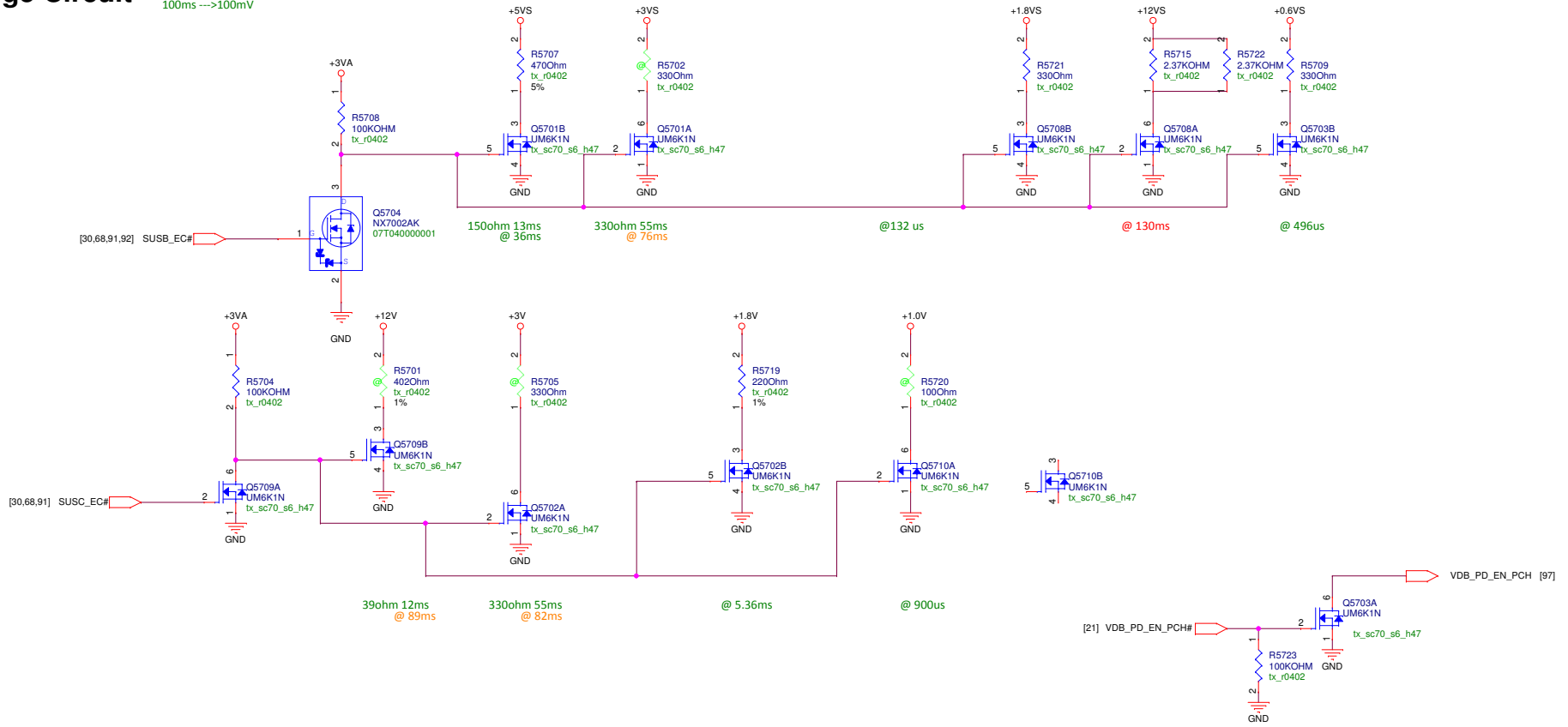


PEGATRON	Title :	IO CONN / POGO PIN	
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer:	Paddy_Ou	
Size: Custom	Project Name: HAWAII		Rev: 0.0
Date: Thursday, March 31, 2016	Sheet 56 of 100		

Discharge Circuit

0402 1/16W min. resister
5V 400 OHM
3V 144 OHM
12V 2304 OHN

100ms --->100mV



+1.0V	+1.0V [7,91]	+0.6VS	+0.6VS [16,17,83]
+1.8V	+1.8V [16,91]	+12VS	+12VS [91]
+3V	+3V [25,91]	+1.8VS	+1.8VS [21,36,45,55,91]
+12V	+12V [91]	+3VS	+3VS [3,4,20,21,22,23,24,30,32,36,40,41,44,45,50,51,53,55,56,62,70,91,92]
+3VA	+3VA [24,30,36,53,56,70,81,93,95]	+5VS	+5VS [36,51,55,56,80,91]

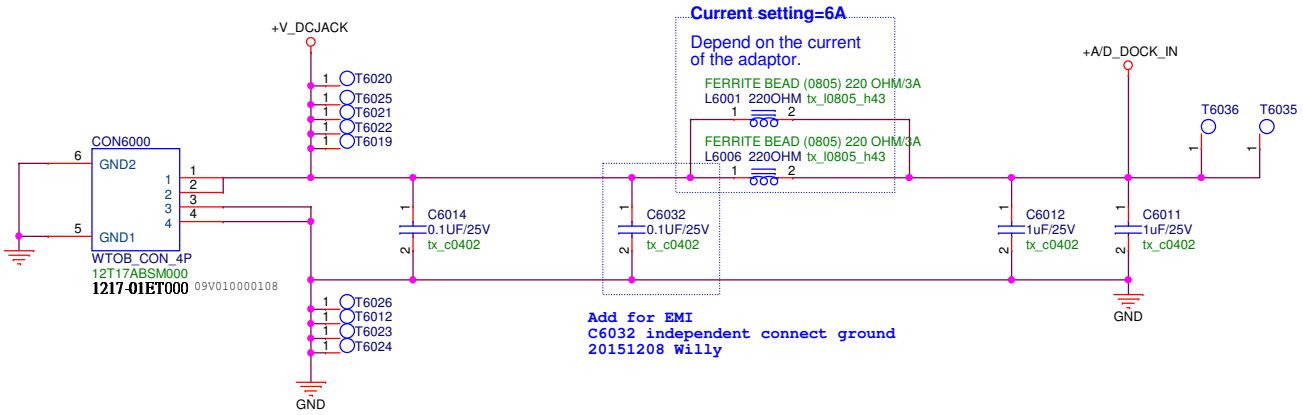
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : DISCHARGE
Engineer: Willy_Liao

Size	Project Name	Rev
Custom	HAWAII	0.0

Date: Thursday, March 31, 2016 Sheet 57 of 100

DC Jack WtoB CONN



+VCC_RTC — +VCC_RTC [24,25,26,36]
+3VA_EC — +3VA_EC [28,30,32]
+3VA — +3VA [24,30,36,53,56,57,70,81,93,95]
+5VA — +5VA [56,81]

+1.0VSUS — +1.0VSUS [26,82]
+1.8VSUS — +1.8VSUS [9,26,84]
+3VSUS — +3VSUS [4,24,25,26,28,30,51,53,62,68,81,84,92,95]
+5VSUS — +5VSUS [52,56,81,84,95,96]
+12VSUS — +12VSUS [81,91]

+3V — +3V [25,57,91]

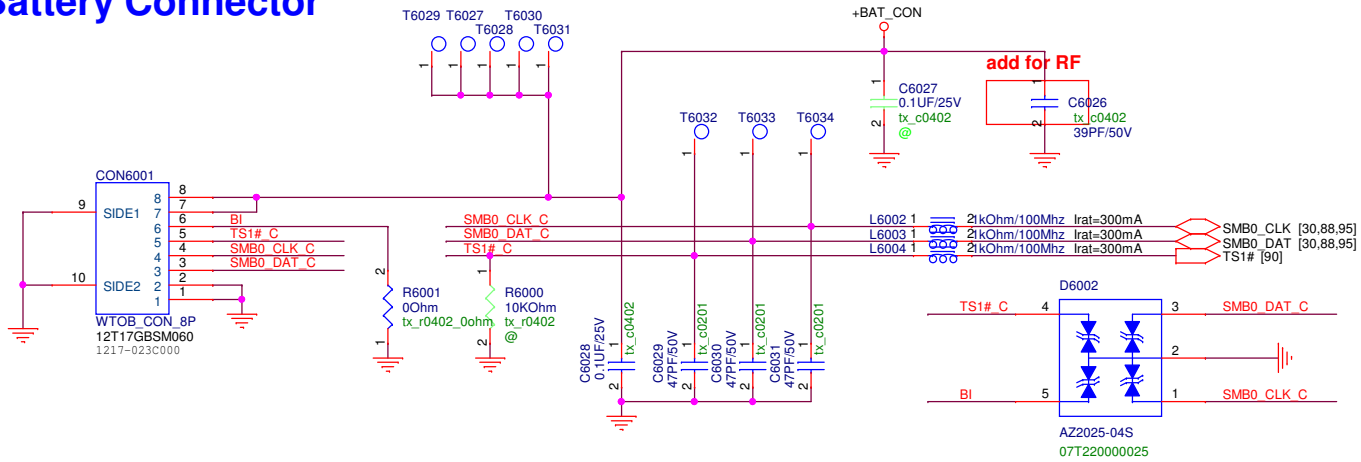
+12V — +12V [57,91]

+1.8VS — +1.8VS [21,36,45,55,57,91]
+3VS — +3VS [3,4,20,21,22,23,24,30,32,36,40,41,44,45,50,51,53,55,56,57,62,70,91,92]
+5VS — +5VS [36,51,55,56,57,80,91]
+12VS — +12VS [57,91]

+AC_BAT_SYS — +AC_BAT_SYS [45,80,81,82,83,88,97]
+A/D_DOCK_IN — +A/D_DOCK_IN [89]
+BAT_CON — +BAT_CON [88]

+VCORE — +VCORE [5,80]
+VCCGT — +VCCGT [6,80]
+VCCSA — +VCCSA [7,80]
+VCCIO — +VCCIO [3,7,9,91]

Battery Connector

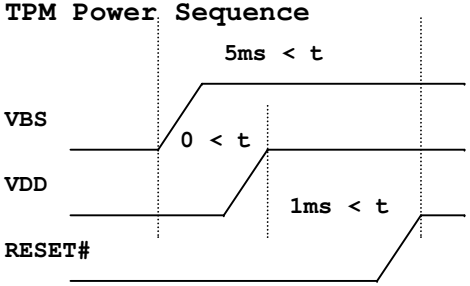


PEGATRON	Title : DC_DC/BAT CONN	
	Engineer: Willy_Liao	
Size: B	Project Name: HAWAII	Rev: 0.0
Date: Thursday, March 31, 2016	Sheet 60 of 100	

TPM

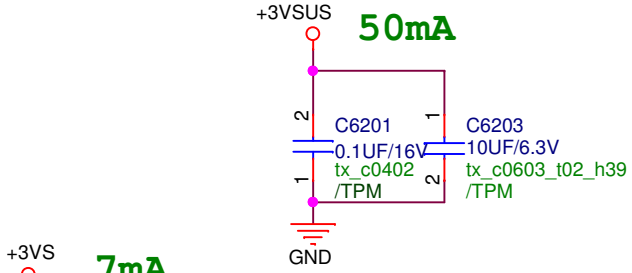
VDD: Power the I/O buffers of the GPIO ports and the Host Interface
VSB: Standby 3.3V Power Supply. Powers the on-chip Core.

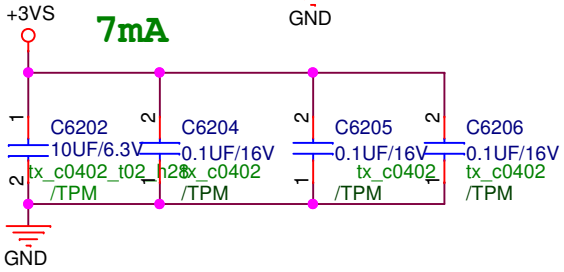
TPM Power Sequence

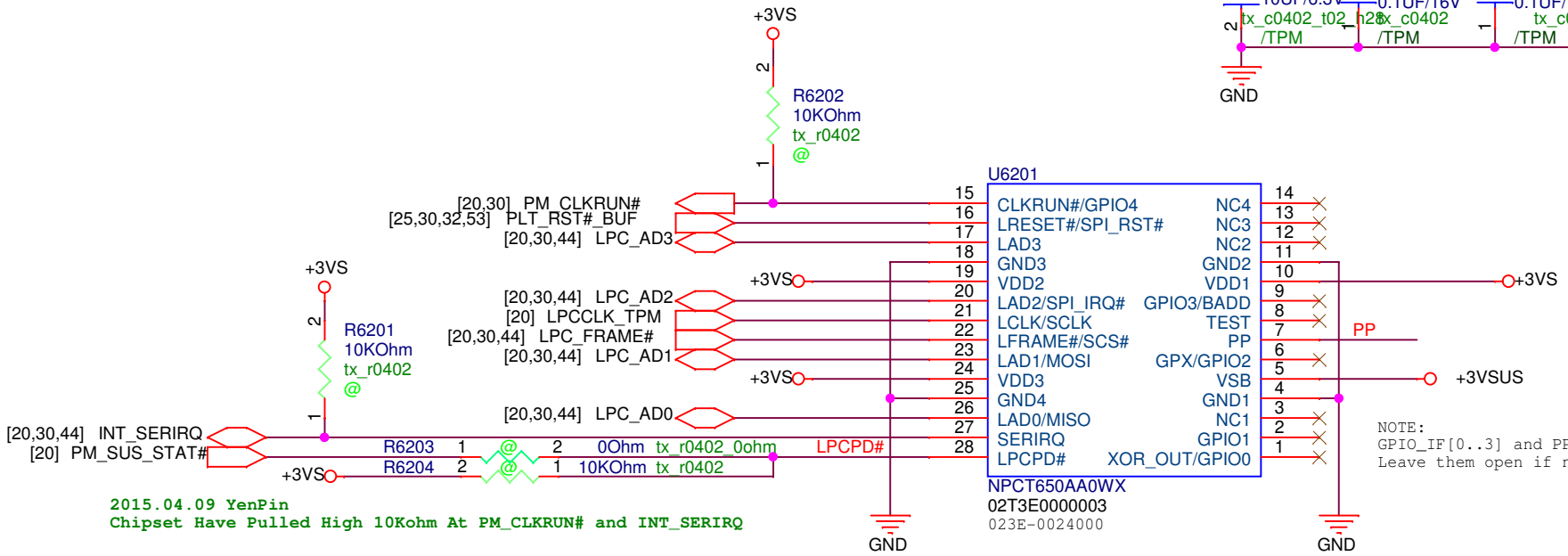


NOTE: RESET# is LRESET#, SPI_RST# or SRESET#.

NOTE:
1) For TPM 1.2:
The TPM VSB pin must be connected to the system's standby voltage (existing at S3 power state).
2) For TPM 2.0:
It is recommended to connect the TPM VSB pin to the system's standby voltage to improve performance.
3) TPM VDD pins should be connected to the same power rail that feeds the Chipset LPC interface.
4) RESET# must be asserted for at least 5 msec after VSB power-up.
5) VSB may come up anytime before VDD power-up, but not after VDD power-up.
6) RESET# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.







NOTE:
GPIO_IF[0..3] and PP are optional.
Leave them open if not used.

2015.04.09 YenPin
Chipset Have Pulled High 10Kohm At PM_CLKRUN# and INT_SERIRQ

NOTE:
1) The PP is an input signal with configurable polarity.
2) By default the PP functionality is disabled.

Note:
When LPCPD# functionality is not required, an internal pull-up resistor allows this pin to be left floating.

PEGATRON

Title : TPM

Engineer: Willy_Liao

Size	Project Name	Rev
A	HAWAII	0.0

Date: Thursday, March 31, 2016 Sheet 62 of 100

[25,30] PM_SUSB# — R6801 1 2 0Ohm tx_r0402_0ohm /BYPAS_EC — SUSB_EC# [30,57,91,92]

[25,30] PM_SUSC# — R6802 1 2 0Ohm tx_r0402_0ohm /BYPAS_EC — SUSC_EC# [30,57,91]

+3VSUS — +3VSUS [4,24,25,26,28,30,51,53,62,81,84,92,95]

For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

Delay By EC(2ms+ EC processing time (3ms~33ms)

[30] DE_ALL_SYS_PGD_EC — R6809 1 2 0Ohm /BYPAS_EC tx_r0402_0ohm — DE_ALL_SYS_PGD_EC_R

delay by EC, delay circuit no longer needed

+3VSUS

U6802
TC7SH08FU
tx_sc70_s5_ti
/BYPAS_EC
06T030000005

PM_SUSB# (pin 2)

R6808 100KOHM tx_r0402 @ — GND

C6804 0.1UF/16V tx_c0402 @ — GND

DE_ALL_SYS_PGD_HW [30]

For shut down Sequence
Tplt17 < 1us

[30] SYS_PWROK_EC — SP6802 0Ohm tx_r0402_short_12mil — SYS_PWROK_EC_G

U6803
TC7SH08FU
tx_sc70_s5_ti
/BYPAS_EC

+3VSUS

For shut down Sequence Tplt17 < 1us
Due to PDG1.2 Figure 43-5. SYS_PWROK drop after PM_SUSB# before CPU_VRON to add this solution

R6804 1 2 0Ohm /BYPAS_EC tx_r0402_0ohm — SYS_PWROK [25,30]

R6806 100KOHM tx_r0402 @ — GND

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

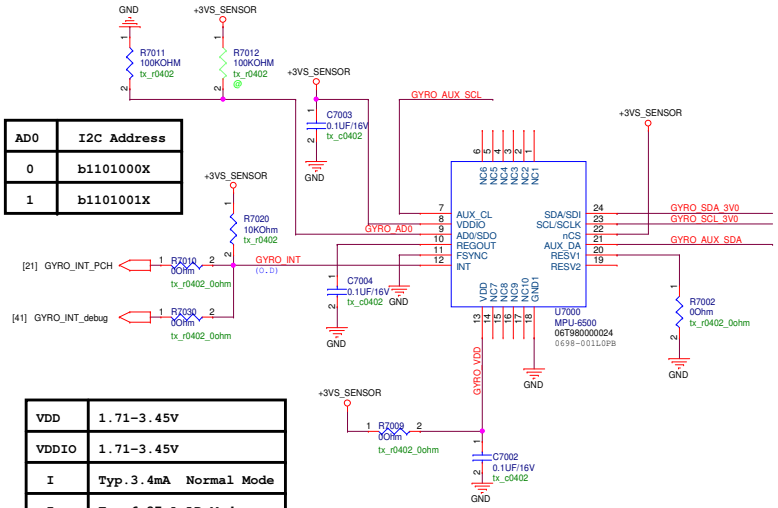
Title : POWER Sequence

Engineer: Willy_Liao

Size	Project Name	Rev
B	HAWAII	0.0

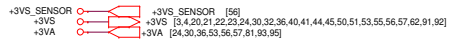
Date: Thursday, March 31, 2016 Sheet 68 of 100

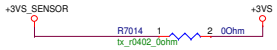
G+G Sensor

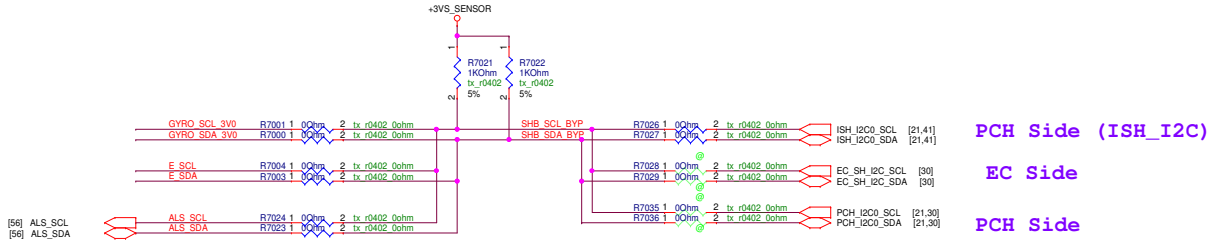


AD0	I2C Address
0	b1101000X
1	b1101001X

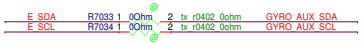
VDD	1.71~3.45V
VDDIO	1.71~3.45V
I	Typ.3.4mA Normal Mode
I	Typ.6.37uA LP Mode

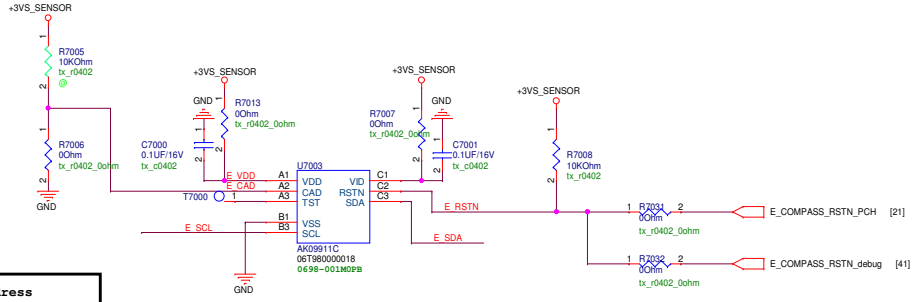






E-Compass

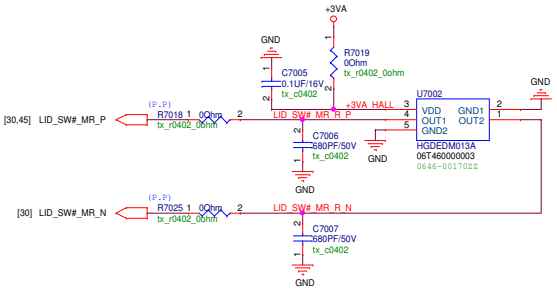


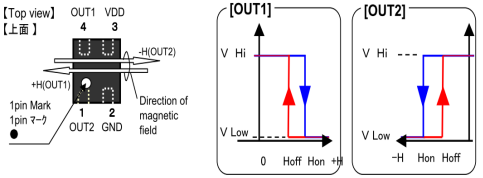


CAD	I2C Address	
1	0xD	PU 10K
0	0xC	PD (default)

VDD	2.4~3.6V
VID	1.65~VDD

MR SENSOR





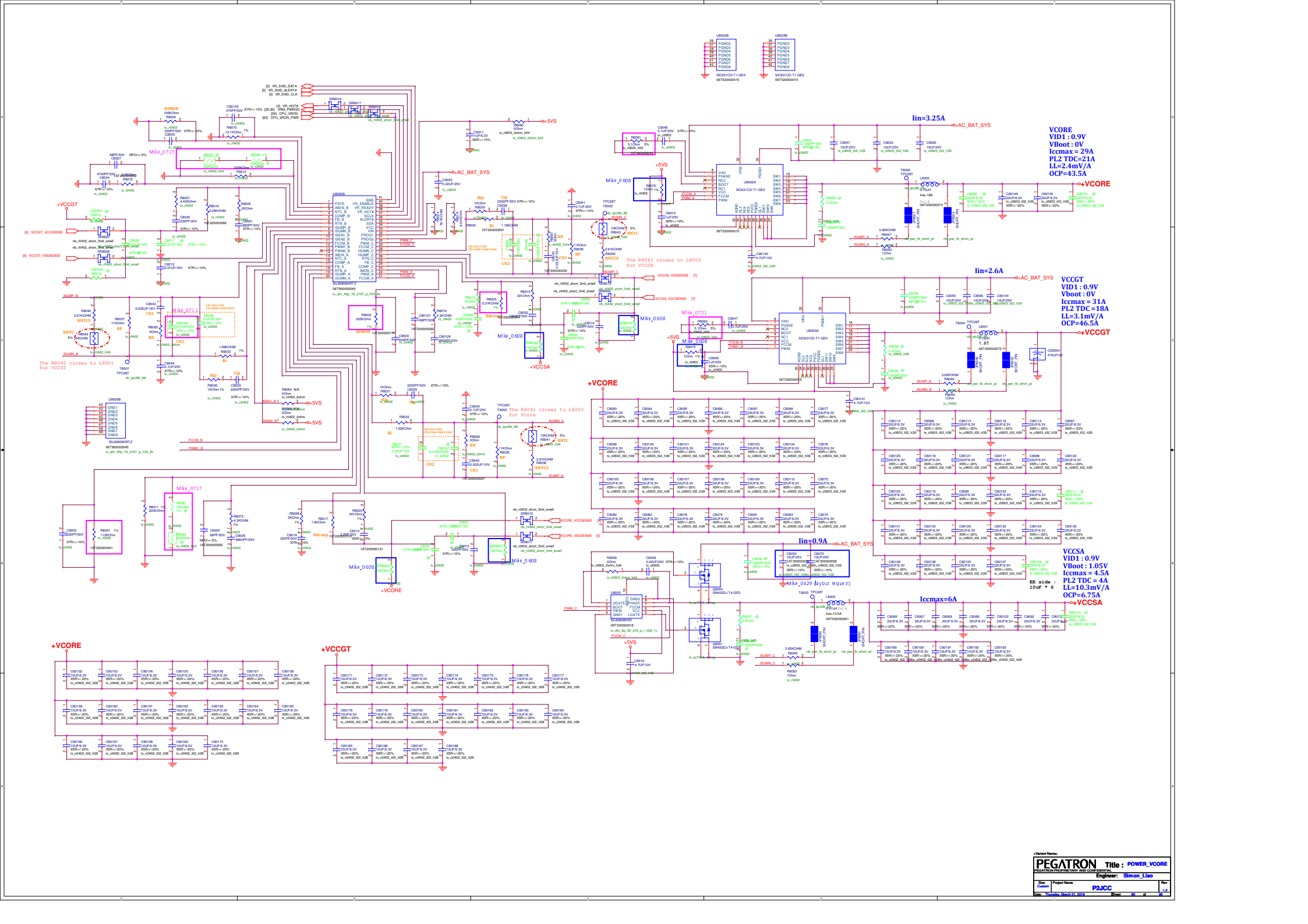
PEGATRON Title : SENSOR

PEGATRON PROPRIETARY AND CONFIDENTIAL

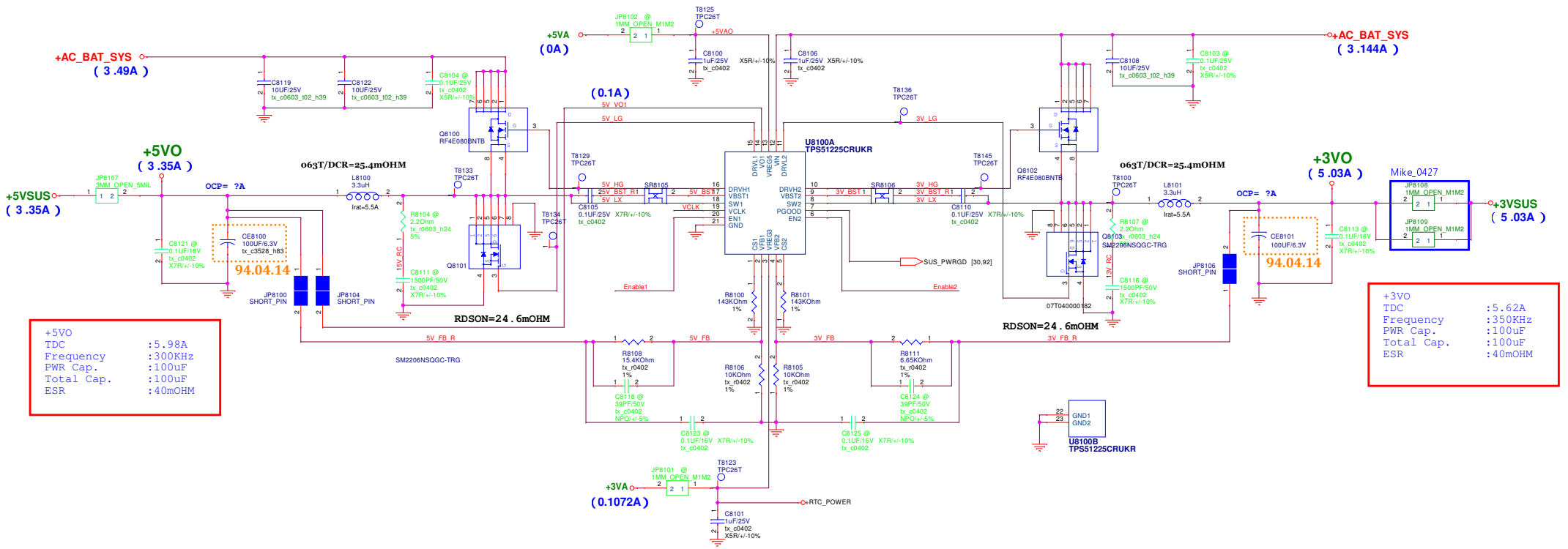
Engineer: Willy_Liao

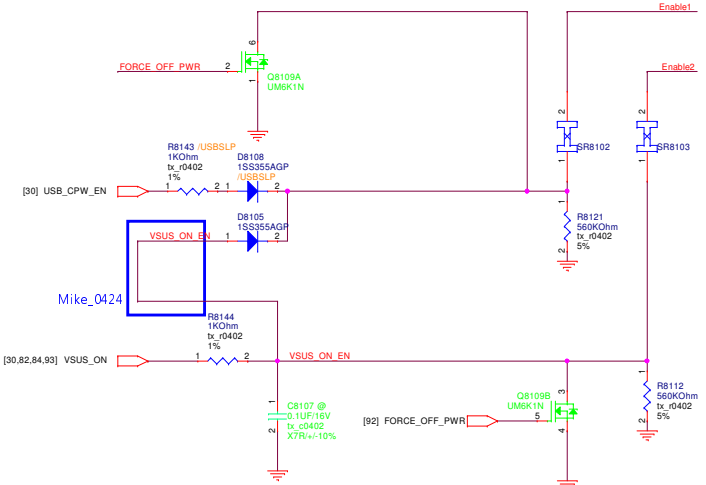
Size	Project Name	Rev
C	HAWAII	0.0

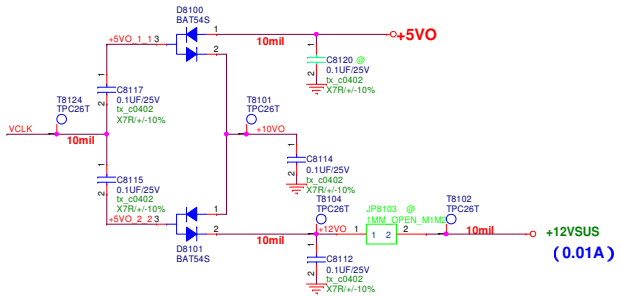
Date: Thursday, March 31, 2016 Sheet 70 of 100

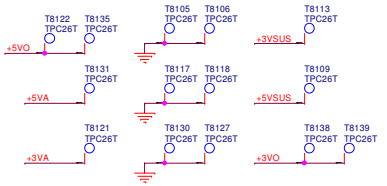

lin=3.25A
VCORE
VID1 : 0.9V
VBoot : 0V
Iccmax = 29A
PL2 TDC=21A
LL=2.4mV/A
OCP=43.5A
+VCORE
lin=2.6A
VCCGT
VID1 : 0.9V
Vboot : 0V
Iccmax = 31A
PL2 TDC =18A
LL=3.1mV/A
OCP=46.5A
+VCCGT
lin=0.9A
VCCSA
VID1 : 0.9V
VBoot : 1.05V
Iccmax = 4.5A
PL2 TDC = 4A
LL=10.3mV/A
OCP=6.75A
+VCCSA
EE side : 10uF * 6
Iccmax=6A
+AC_BAT_SYS
+5VS
+VCCSA
The R8042 closes to L8001 for VCCGT
The R8043 closes to L8002 for VCCSA
The R8041 closes to L8000 for Vcore
Mike_0717
Mike_0713
Mike_0608
Mike_0721
Mike_0429 (layout request)
PEGATRON
Title : POWER_VCORE
Engineer: Simon_Liao
P2JCC
Thursday, March 31, 2016

+5VO & +3VO POWER SUPPLY



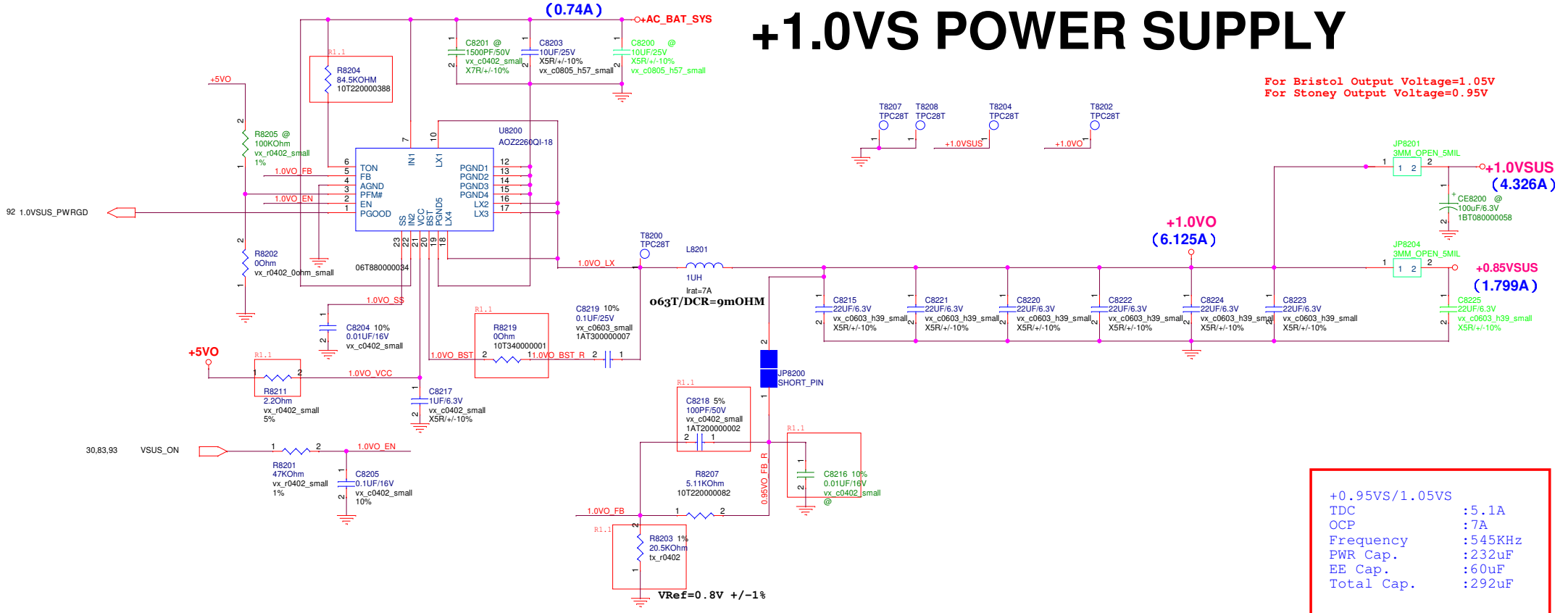






<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_SYSTEM
Engineer: Simon_Liao
Size Custom
Project Name P2JCC
Rev 1.0
Date: Thursday, March 31, 2016
Sheet 81 of 96

+1.0VS POWER SUPPLY



For Bristol Output Voltage=1.05V
For Stoney Output Voltage=0.95V

+0.95VS/1.05VS	
TDC	:5.1A
OCP	:7A
Frequency	:545KHz
PWR Cap.	:232uF
EE Cap.	:60uF
Total Cap.	:292uF

For Bristol R8207=6.2KOHM(10V220000088), Output Voltage=1.05V
For Stoney R8207=3.74KOHM(10V220000233), Output Voltage=0.95V

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

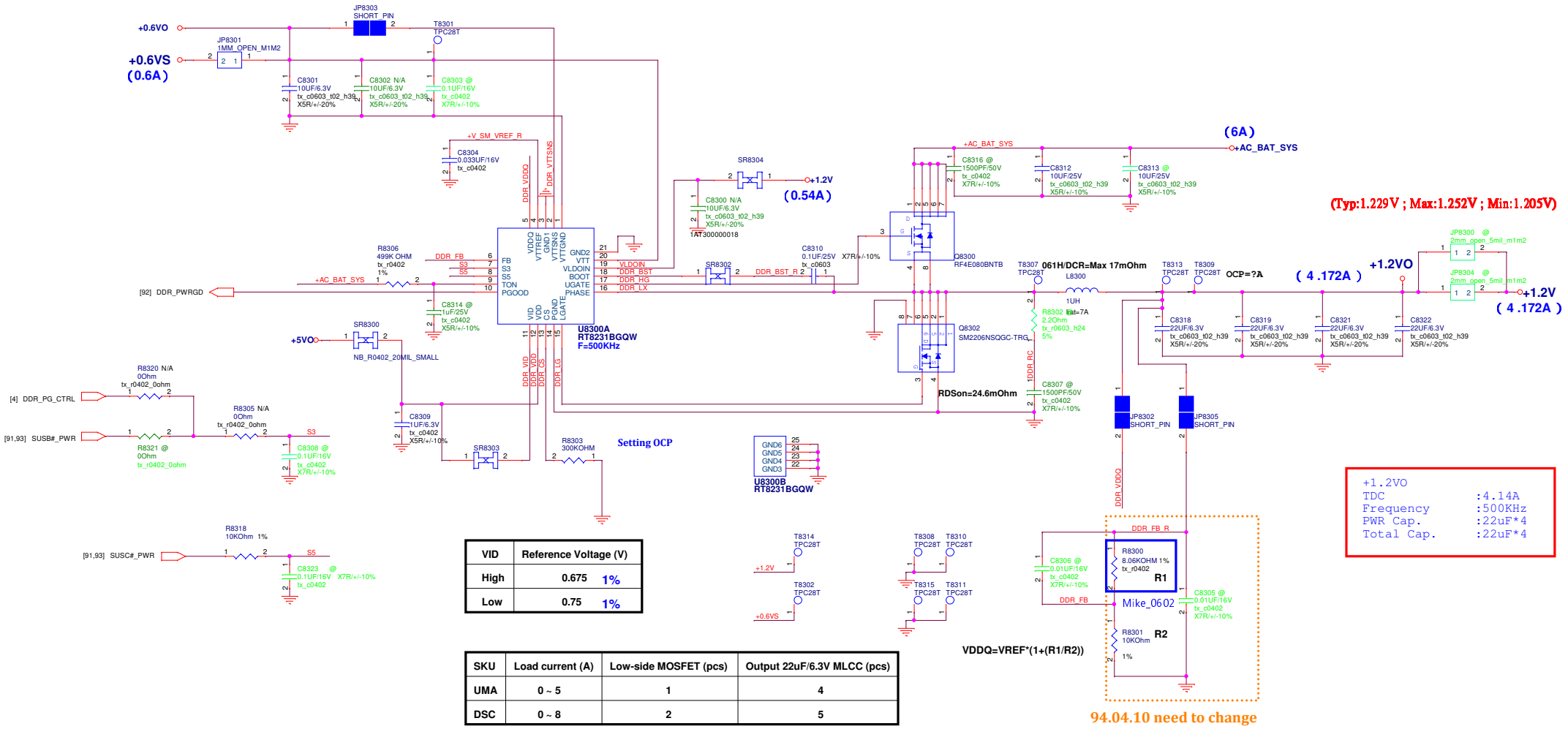
Title : +0.95VS/+1.0VS

Engineer: Simon_Liao

Size	Project Name	Rev
Custom	P2JCC	1.0

Date: Thursday, March 31, 2016 Sheet 82 of 96

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675 1%
Low	0.75 1%

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON PROPRIETARY AND CONFIDENTIAL

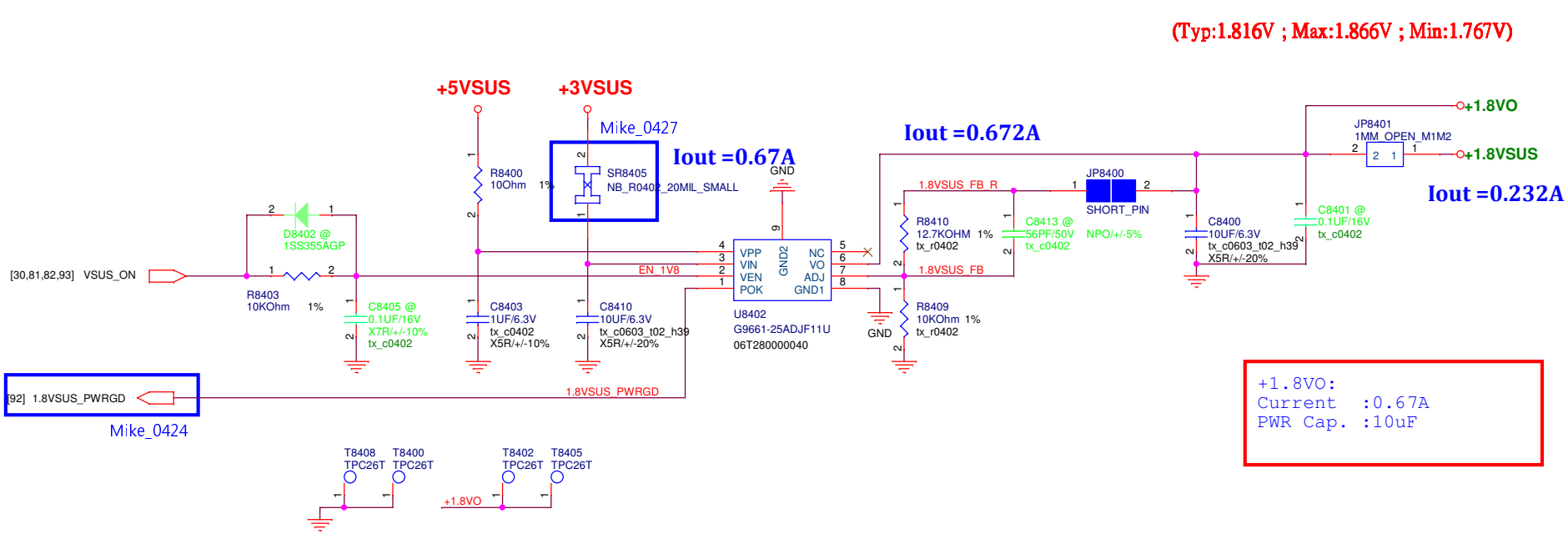
Title : POWER_DDR & VTT

Engineer: Simon_Liao

Size: Custom | Project Name: P2JCC | Rev: 1.0

Date: Thursday, March 31, 2016 | Sheet 83 of 96

1.8VSUS POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

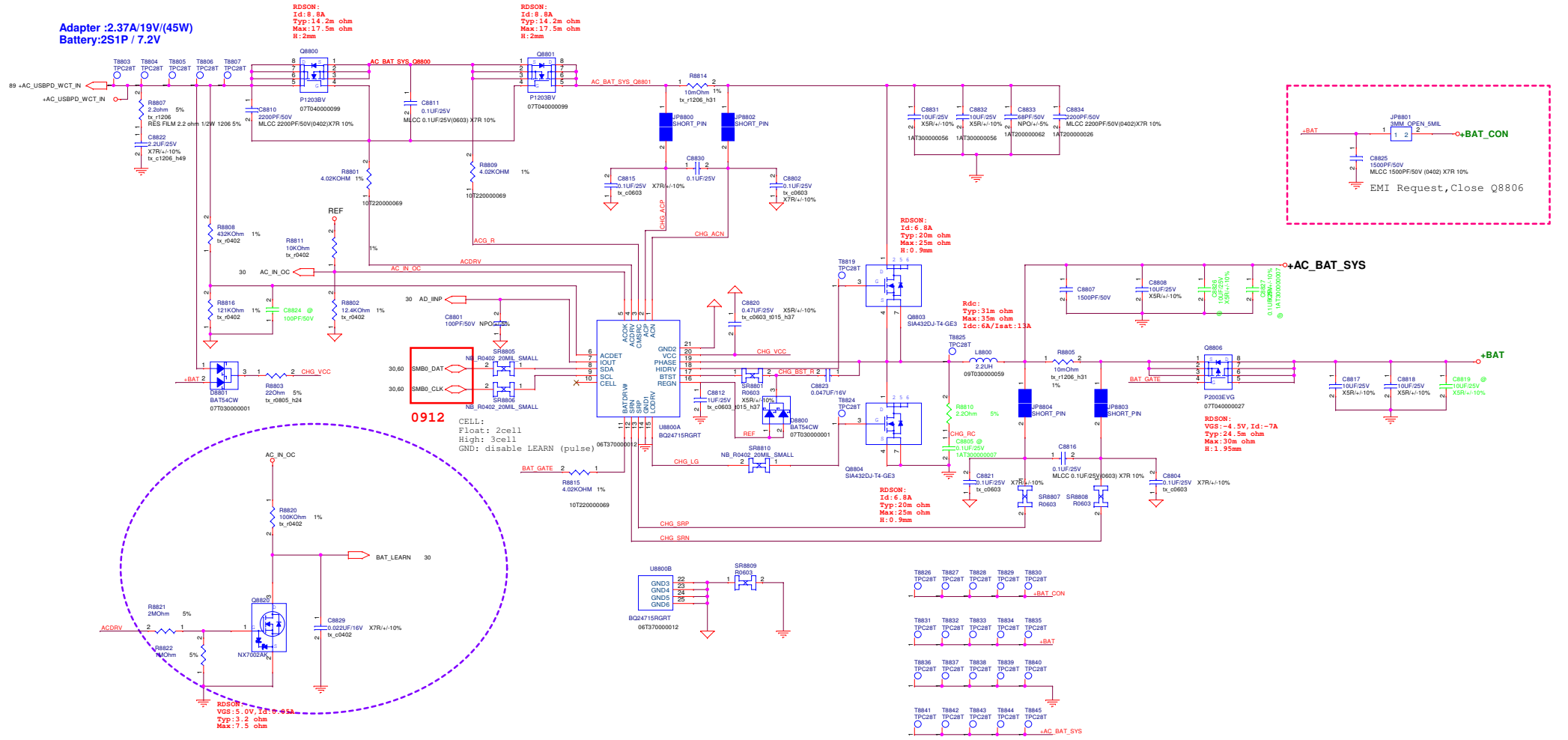
Title : PAGE 84 POWER

Engineer: Simon_Liao

Size	Project Name	Rev
B	P2JCC	1.0

Date: Thursday, March 31, 2016 Sheet 84 of 96

BQ24715_NVDC BATTERY CHARGER

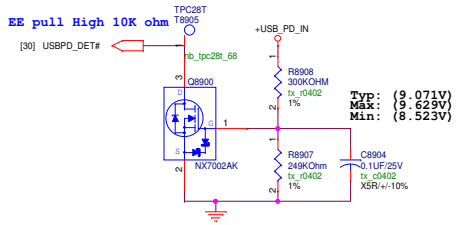


<Variant Name>

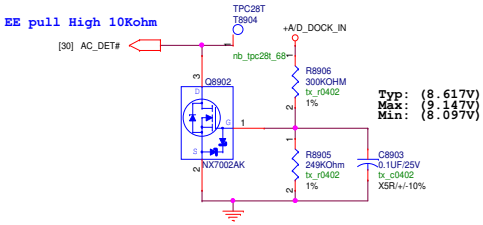
PEGATRON Title : POWER_CHARGER
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Simon_Liao
Size: Custom | Project Name: P2JCC | Rev: 1.0
Date: Thursday, March 31, 2016 | Sheet 88 of 94

AC & USB_PD & Wireless Charger Detect

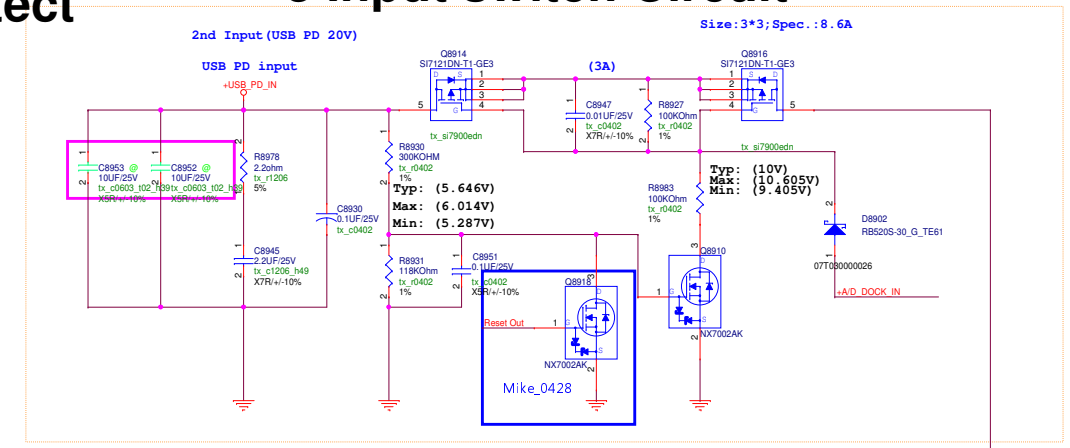
+USB PD_IN DETECT 45W(5V-20V)

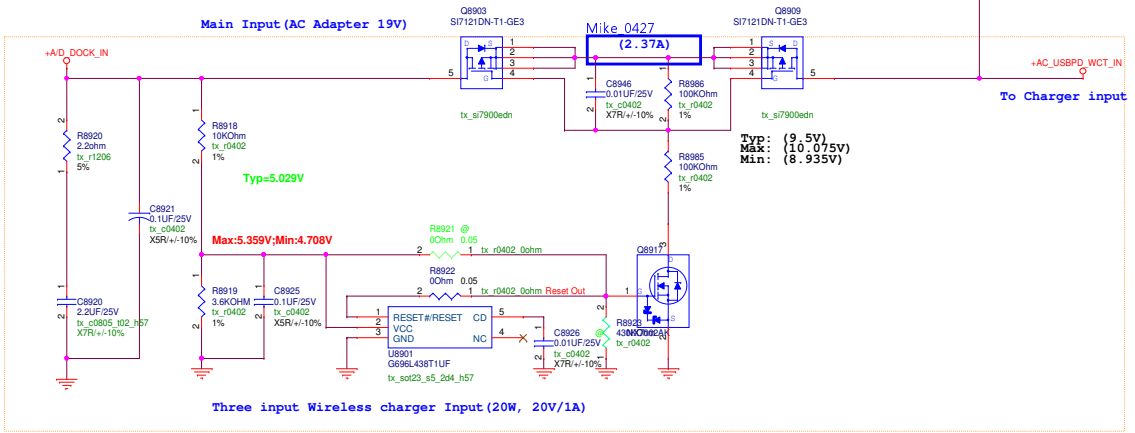


+AC_IN DETECT(45W,19V)



3 Input switch Circuit



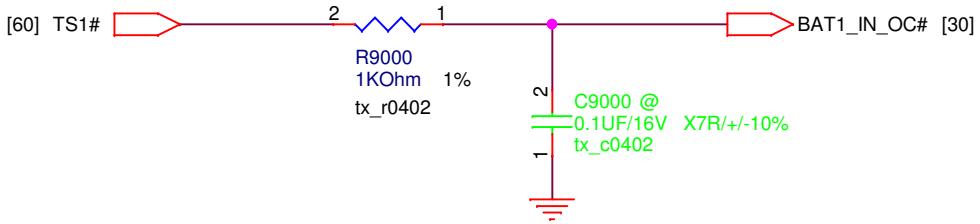


Three input Wireless charger Input(20W, 20V/1A)

USBPD_DET#	AC_DET#	WCT_DET#	WCT_EN	BQ24715 Charger EN DAT&CLK	DPM	Power Limit
0	0	0	L	H	AC_Adapter	45W*90%
0	0	1	L	H	AC_Adapter	45W*90%
0	1	0	L	H	USB_PD	45W*90%??
0	1	1	L	H	USB_PD	45W*90%??
1	0	0	L	H	AC_Adapter	45W*90%
1	0	1	L	H	AC_Adapter	45W*90%
1	1	0	L	H	WCT	20W*90%
1	1	1	X	X	X	X

PEGATRON Title : AC&PD&Wireless S.W.
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Simon_Liao
Size C | Project Name P2JCC | Rev 1.0
Date: Thursday, March 31, 2016 | Sheet 89 of 96

BATTERY IN DETECT



<Variant Name>

PEGATRON

Title : POWER_DETECT

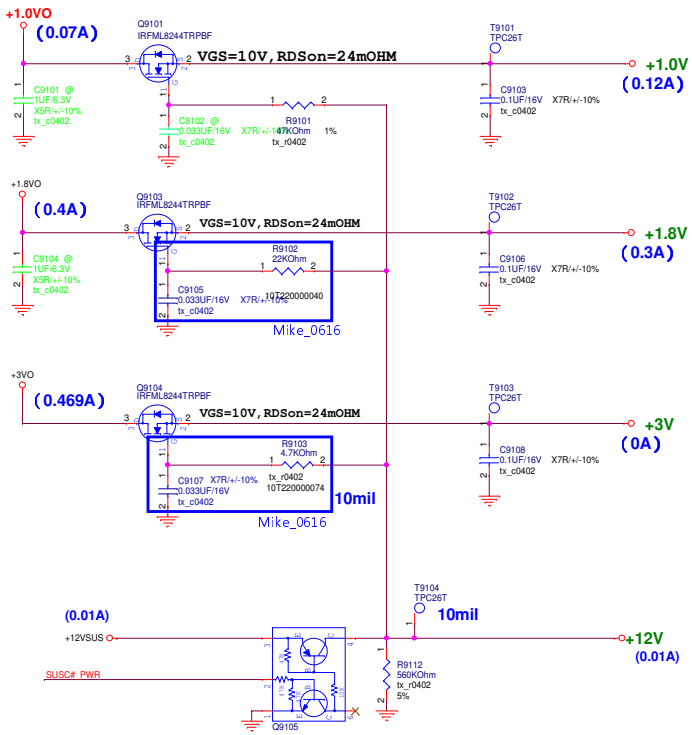
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Simon_Liao

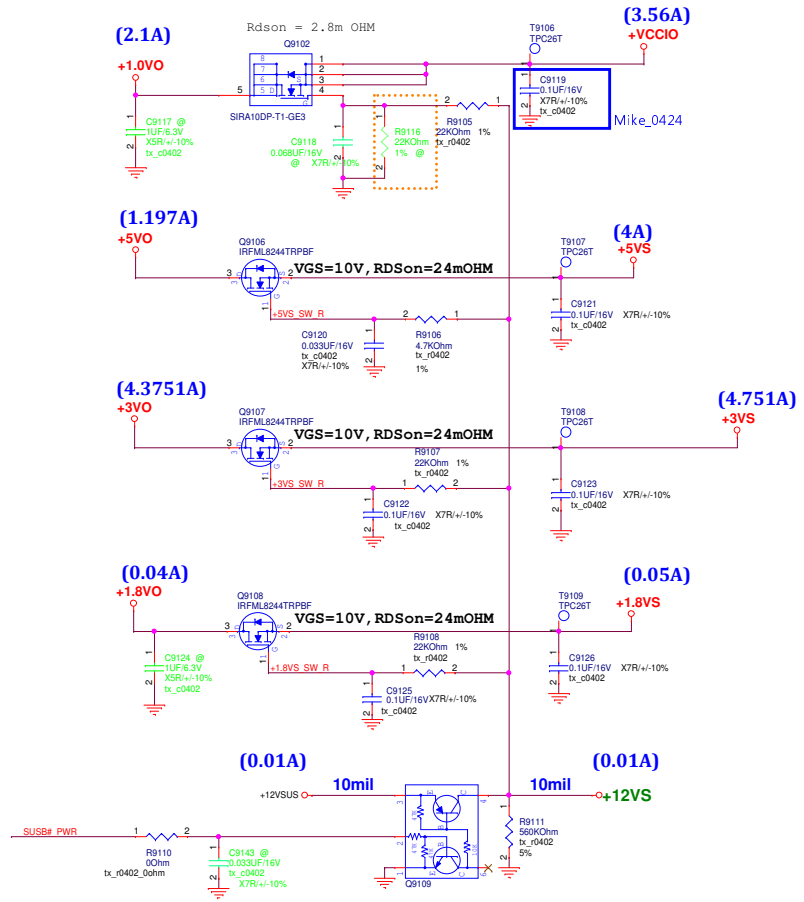
Size	Project Name	Rev
A	P2JCC	1.0

Date: Thursday, March 31, 2016 Sheet 90 of 96

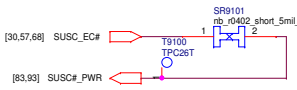
SUSC#_PWR POWER



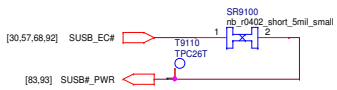
SUSB#_PWR POWER



SUSC#_PWR POWER Control



SUSB#_PWR POWER Control



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

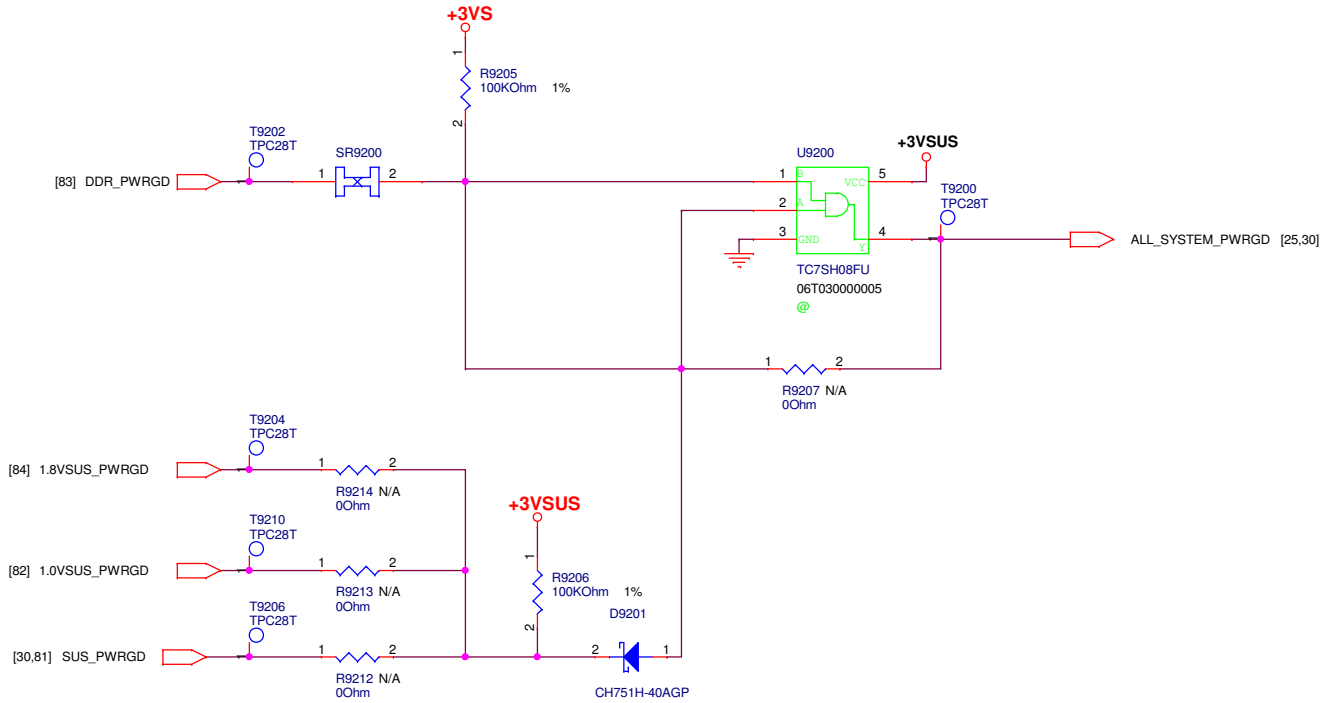
Title : POWER_LOAD SWITCH

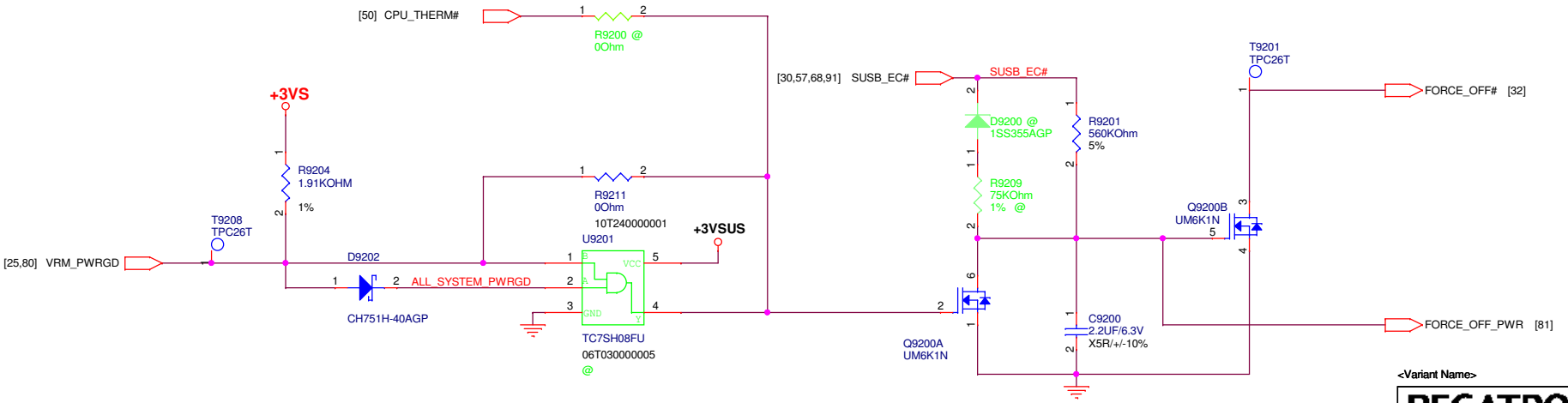
Engineer: Simon_Liao

Size	Project Name	Rev
C	P2JCC	1.0

Date: Thursday, March 31, 2016 Sheet 91 of 96

POWER GOOD DETECTER





<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

Engineer: Simon_Liao

Size	Project Name	Rev
Custom	P2JCC	1.0

Date: Thursday, March 31, 2016 Sheet 92 of 96

+AC_USBPD_WCT_IN → +AC_USBPD_WCT_IN 88

+AC_BAT_SYS → +AC_BAT_SYS 80,81,83,87,88

+BAT_CON → +BAT_CON 88

+BAT → +BAT 88

+5VA → +5VA 81

+3VA → +3VA 81,88

+5VO → +5VO 81,83,91

+3VO → +3VO 81,82,84,86,91

+1.8VO → +1.8VO 84

+1.2VO → +1.2VO 83,91

+1.0VO → +1.0VO 82

+0.6VO → +0.6VO 83

+12VSUS → +12VSUS 81,91

+5VSUS → +5VSUS 81

+3VSUS → +3VSUS 81,92

+3V → +3V 91

+1.2V → +1.2V 83

+12VS → +12VS 91

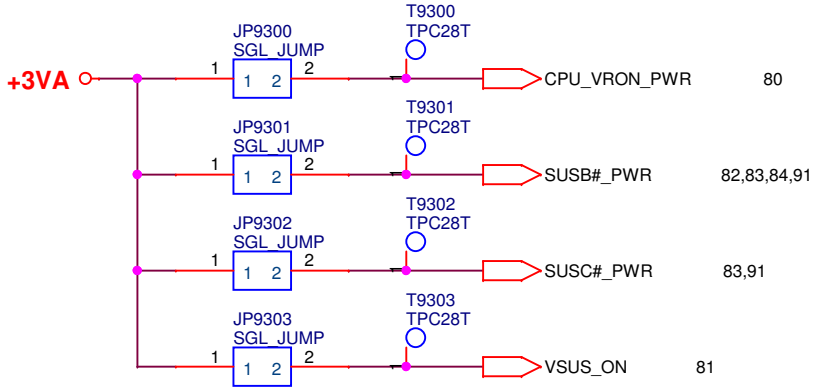
+5VS → +5VS 80,87,91

+3VS → +3VS 80,91,92

+0.6VS → +0.6VS 83

+VCORE → +VCORE 80

FOR POWER TEST



<Variant Name>

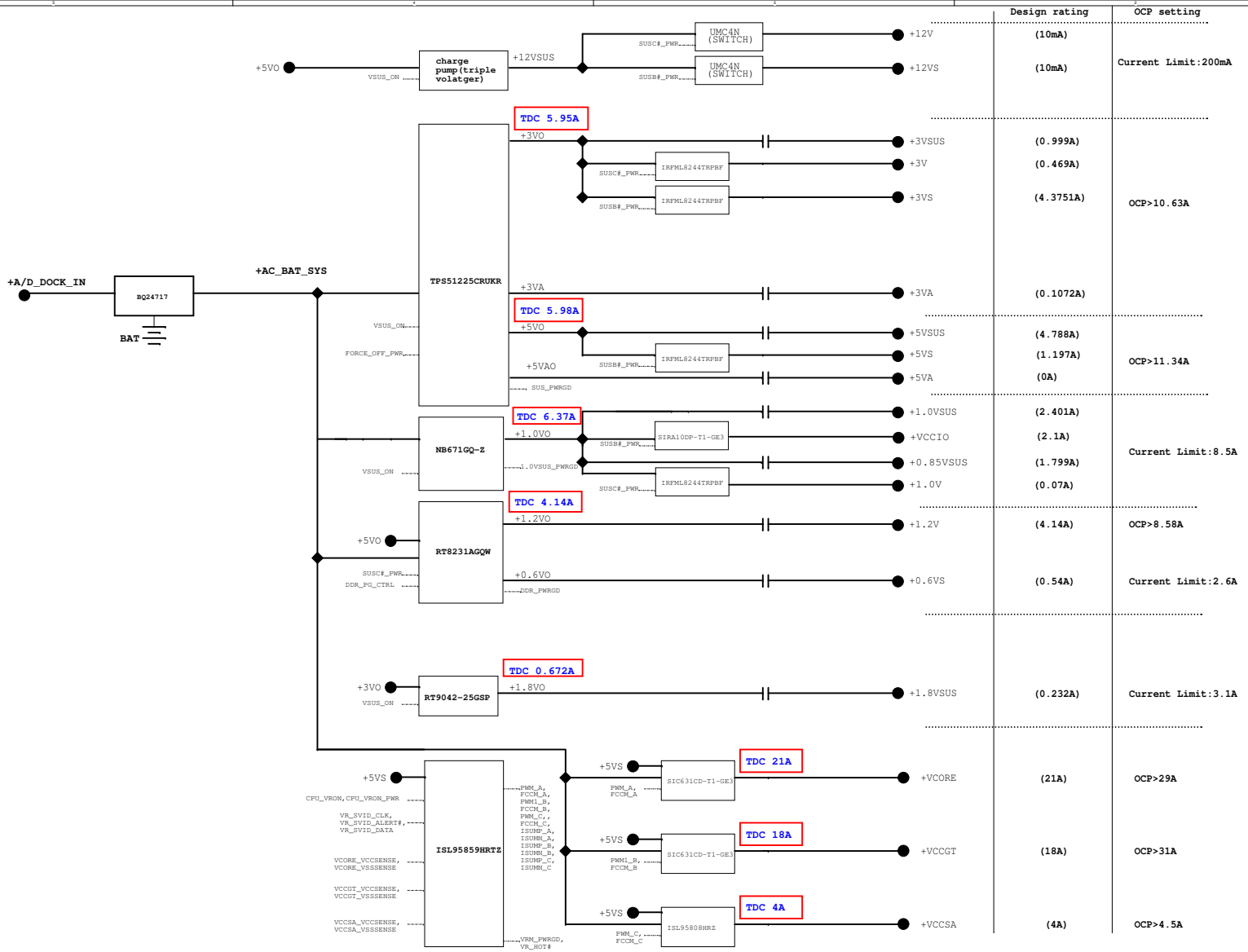
PEGATRON Title : POWER_SIGNAL

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Simon_Liao

Size	Project Name	Rev
Custom	P2JCC	1.0

Date: Thursday, March 31, 2016 Sheet 93 of 96



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

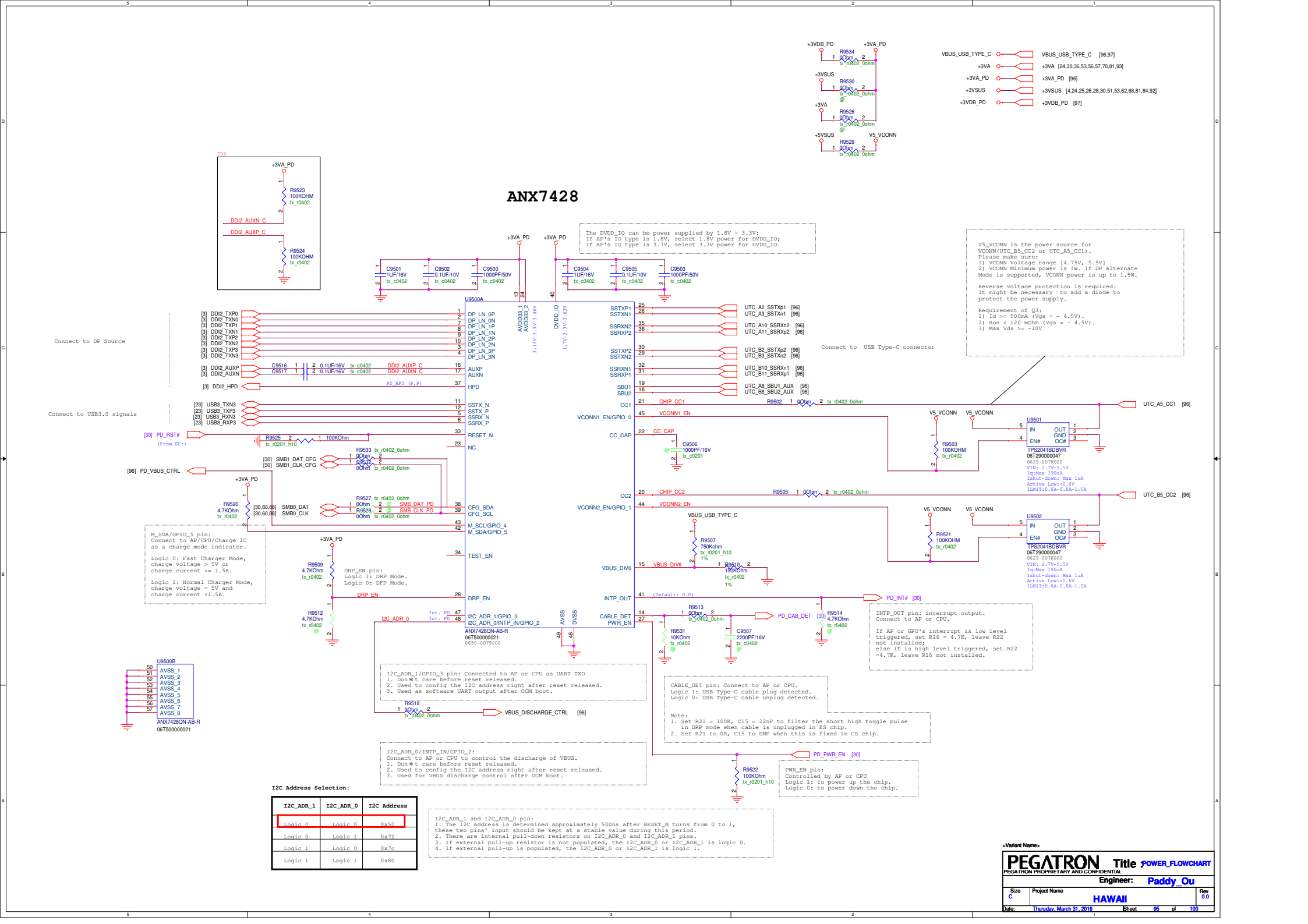
Title : POWER_FLOWCHART

Engineer: Simon_Liao

Size	Project Name	Rev
D	P2JCC	1.0

Date: Thursday, March 31, 2016 Sheet 94 of 96

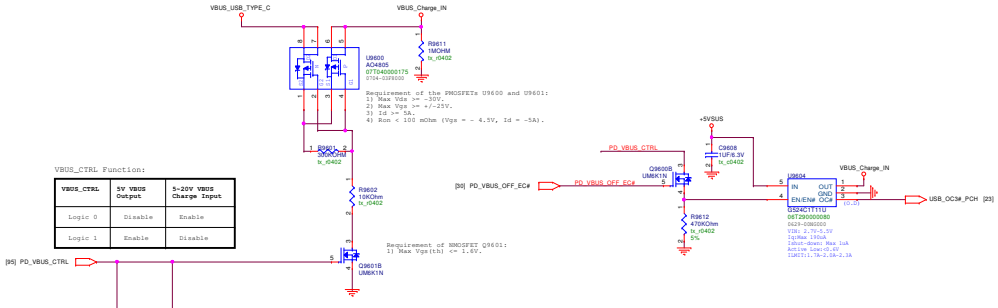
ANX7428


+3VDB_PD
+3VA_PD
R9534 0Ohm tx_r0402_0ohm
+3VSUS
R9530 0Ohm tx_r0402_0ohm @
+3VA
R9526 0Ohm tx_r0402_0ohm @
+5VSUS
V5_VCONN
R9529 0Ohm tx_r0402_0ohm
VBUS_USB_TYPE_C [96,97]
+3VA [24,30,36,53,56,57,70,81,93]
+3VA_PD [96]
+3VSUS [4,24,25,26,28,30,51,53,62,68,81,84,92]
+3VDB_PD [97]
TBD
R9523 100KOHM tx_r0402
DDI2_AUXN_C
DDI2_AUXP_C
R9524 100KOHM tx_r0402
U9500A
C9501 1UF/16V tx_c0402
C9502 0.1UF/10V tx_c0402
C9500 1000PF/50V tx_c0402
C9504 1UF/16V tx_c0402
C9505 0.1UF/10V tx_c0402
C9503 1000PF/50V tx_c0402
AVDD33_1
AVDD33_2
3.14V~3.3V~3.46V
DVDD_IO
1.7V~3.3V~3.63V
The DVDD_IO can be power supplied by 1.8V ~ 3.3V:
If AP's IO type is 1.8V, select 1.8V power for DVDD_IO;
If AP's IO type is 3.3V, select 3.3V power for DVDD_IO.
V5_VCONN is the power source for VCONN(UTC_B5_CC2 or UTC_A5_CC1).
Please make sure:
1) VCONN Voltage range [4.75V, 5.5V]
2) VCONN Minimum power is 1W. If DP Alternate Mode is supported, VCONN power is up to 1.5W.
Reverse voltage protection is required.
It might be necessary to add a diode to protect the power supply.
Requirement of Q3:
1) Id >= 500mA (Vgs = - 4.5V).
2) Ron < 120 mOhm (Vgs = - 4.5V).
3) Max Vds >= -10V
Connect to DP Source
[3] DDI2_TXP0
[3] DDI2_TXN0
[3] DDI2_TXP1
[3] DDI2_TXN1
[3] DDI2_TXP2
[3] DDI2_TXN2
[3] DDI2_TXP3
[3] DDI2_TXN3
DP_LN_0P
DP_LN_0N
DP_LN_1P
DP_LN_1N
DP_LN_2P
DP_LN_2N
DP_LN_3P
DP_LN_3N
C9516 0.1UF/16V tx_c0402 DDI2_AUXP_C
C9517 0.1UF/16V tx_c0402 DDI2_AUXN_C
[3] DDI2_AUXP
[3] DDI2_AUXN
AUXP
AUXN
[3] DDI2_HPD
PD_HPD (P.P)
HPD
Connect to USB3.0 signals
[23] USB3_TXN3
[23] USB3_TXP3
[23] USB3_RXN3
[23] USB3_RXP3
SSTX_N
SSTX_P
SSRX_N
SSRX_P
[30] PD_RST#
(From EC:)
R9525 100KOhm tx_r0201_h10
RESET_N
NC
[30] SMB1_DAT_CFG
[30] SMB1_CLK_CFG
R9533 0Ohm tx_r0402_0ohm
R9532 0Ohm tx_r0402_0ohm
[96] PD_VBUS_CTRL
+3VA_PD
R9520 4.7KOhm tx_r0402
[30,60,88] SMB0_DAT
[30,60,88] SMB0_CLK
R9527 0Ohm tx_r0402_0ohm @ SMB_DAT_PD
R9528 0Ohm tx_r0402_0ohm @ SMB_CLK_PD
CFG_SDA
CFG_SCL
M_SCL/GPIO_4
M_SDA/GPIO_5
M_SDA/GPIO_5 pin:
Connect to AP/CPU/Charge IC as a charge mode indicator.
Logic 0: Fast Charger Mode, charge voltage > 5V or charge current >= 1.5A.
Logic 1: Normal Charger Mode, charge voltage = 5V and charge current <1.5A.
TEST_EN
+3VA_PD
R9509 4.7KOhm tx_r0402
DRP_EN pin:
Logic 1: DRP Mode.
Logic 0: DFP Mode.
DRP_EN
DRP_EN
R9512 4.7KOhm tx_r0402 @
I2C_ADR_0
Int. PD
Int. PD
I2C_ADR_1/GPIO_3
I2C_ADR_0/INTP_IN/GPIO_2
ANX7428QN-AB-R
06T500000021
0650-0079000
AVSS
DVSS
I2C_ADR_1/GPIO_3 pin: Connected to AP or CPU as UART TXD
1. Don*t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used as software UART output after OCM boot.
R9518 0Ohm tx_r0402_0ohm
VBUS_DISCHARGE_CTRL [96]
I2C_ADR_0/INTP_IN/GPIO_2:
Connect to AP or CPU to control the discharge of VBUS.
1. Don*t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used for VBUS discharge control after OCM boot.
U9500B
AVSS_1
AVSS_2
AVSS_3
AVSS_4
AVSS_5
AVSS_6
AVSS_7
AVSS_8
ANX7428QN-AB-R
06T500000021
I2C Address Selection:
I2C_ADR_1 | I2C_ADR_0 | I2C Address
Logic 0 | Logic 0 | 0x50
Logic 0 | Logic 1 | 0x72
Logic 1 | Logic 0 | 0x7c
Logic 1 | Logic 1 | 0x80
I2C_ADR_1 and I2C_ADR_0 pin:
1. The I2C address is determined approximately 500ns after RESET_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C_ADR_0 and I2C_ADR_1 pins.
3. If external pull-up resistor is not populated, the I2C_ADR_0 or I2C_ADR_1 is logic 0.
4. If external pull-up is populated, the I2C_ADR_0 or I2C_ADR_1 is logic 1.
Connect to USB Type-C connector
SSTXP1
SSTXN1
SSRXN2
SSRXP2
SSTXP2
SSTXN2
SSRXN1
SSRXP1
SBU1
SBU2
UTC_A2_SSTXp1 [96]
UTC_A3_SSTXn1 [96]
UTC_A10_SSRXn2 [96]
UTC_A11_SSRXp2 [96]
UTC_B2_SSTXp2 [96]
UTC_B3_SSTXn2 [96]
UTC_B10_SSRXn1 [96]
UTC_B11_SSRXp1 [96]
UTC_A8_SBU1_AUX [96]
UTC_B8_SBU2_AUX [96]
CC1
CHIP_CC1
R9502 0Ohm tx_r0402_0ohm
UTC_A5_CC1 [96]
VCONN1_EN/GPIO_0
VCONN1_EN
CC_CAP
CC_CAP
C9506 1000PF/16V tx_c0201
V5_VCONN
R9503 100KOHM tx_r0402
U9501
IN
EN#
OUT
GND
OC#
TPS2041BDBVR
06T290000047
0629-007K000
VIN: 2.7V~5.5V
Iq:Max 190uA
Ishut-down: Max 1uA
Active Low:<0.6V
ILMIT:0.6A~0.8A~1.0A
CC2
CHIP_CC2
R9505 0Ohm tx_r0402_0ohm
UTC_B5_CC2 [96]
VCONN2_EN/GPIO_1
VCONN2_EN
VBUS_USB_TYPE_C
R9507 750Kohm tx_r0201_h10 1%
VBUS_DIV6
VBUS_DIV6
R9510 150KOhm tx_r0402 1%
R9521 100KOHM tx_r0402
U9502
TPS2041BDBVR
06T290000047
0629-007K000
INTP_OUT
(Default: O.D)
PD_INT# [30]
R9513 0Ohm tx_r0402_0ohm
INTP_OUT pin: interrupt output.
Connect to AP or CPU.
If AP or GPU's interrupt is low level triggered, set R16 = 4.7K, leave R22 not installed;
else if is high level triggered, set R22 =4.7K, leave R16 not installed.
CABLE_DET
PWR_EN
PD_CAB_DET [30]
R9514 4.7KOhm tx_r0402 @
R9531 10KOhm tx_r0402 @
C9507 2200PF/16V tx_c0402 @
CABLE_DET pin: Connect to AP or CPU.
Logic 1: USB Type-C cable plug detected.
Logic 0: USB Type-C cable unplug detected.
Note:
1. Set R21 = 100K, C15 = 22nF to filter the short high toggle pulse in DRP mode when cable is unplugged in ES chip.
2. Set R21 to 0R, C15 to DNP when this is fixed in CS chip.
PD_PWR_EN [30]
R9522 100KOhm tx_r0201_h10
PWR_EN pin:
Controlled by AP or CPU
Logic 1: to power up the chip.
Logic 0: to power down the chip.
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_FLOWCHART
Engineer: Paddy_Ou
Size C
Project Name HAWAII
Rev 0.0
Date: Thursday, March 31, 2016
Sheet 95 of 100

VBUS Control

Optional:
If PMIC can detect VBUS presence and disable/enable VBUS, the VBUS control circuit can be removed.

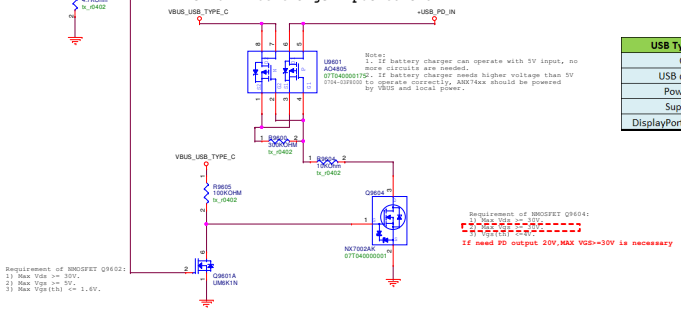
5V VBUS Output Control



VBUS_CTRL Function:

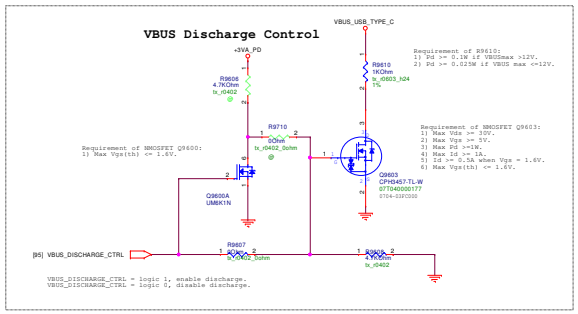
VBUS_CTRL	5V VBUS Output	5~20V VBUS Charge Input
Logic 0	Disable	Enable
Logic 1	Enable	Disable

5~20V VBUS Charge Input Control



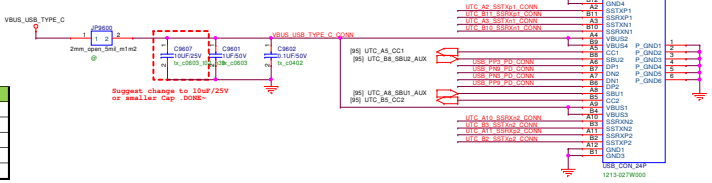
USB Type C features	On Hawaii
CC logic	Yes
USB data transfer	ANX7428: USB 3.1 Gen1 (5Gbit/s), SOC: USB 3.0
Power Delivery	5V/2.25A(Cannot charge when dead battery), 12V/2.25A, 19.6V/2.25A
Support Power	5V/1.5A
DisplayPort Alternative Mode	ANX7428: DP1.3, SOC: DP1.3

VBUS Discharge Control

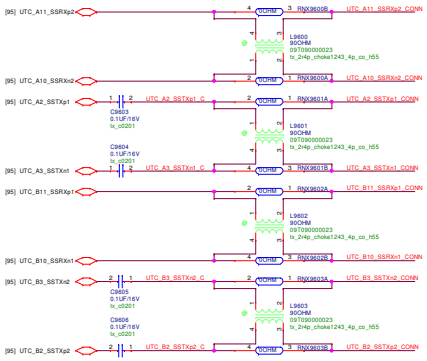


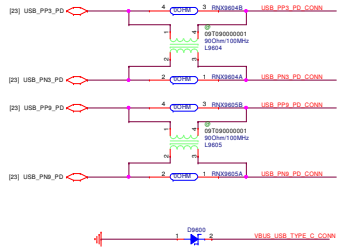
USB Type C Connector

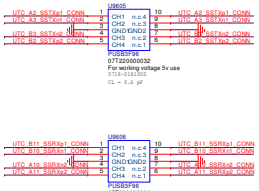
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

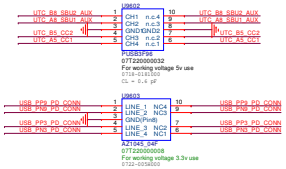


ESD









<variant_name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_FLOWCHART

Engineer: Paddy_Ou

Size	Project Name	Rev
D	HAWAII	0.0

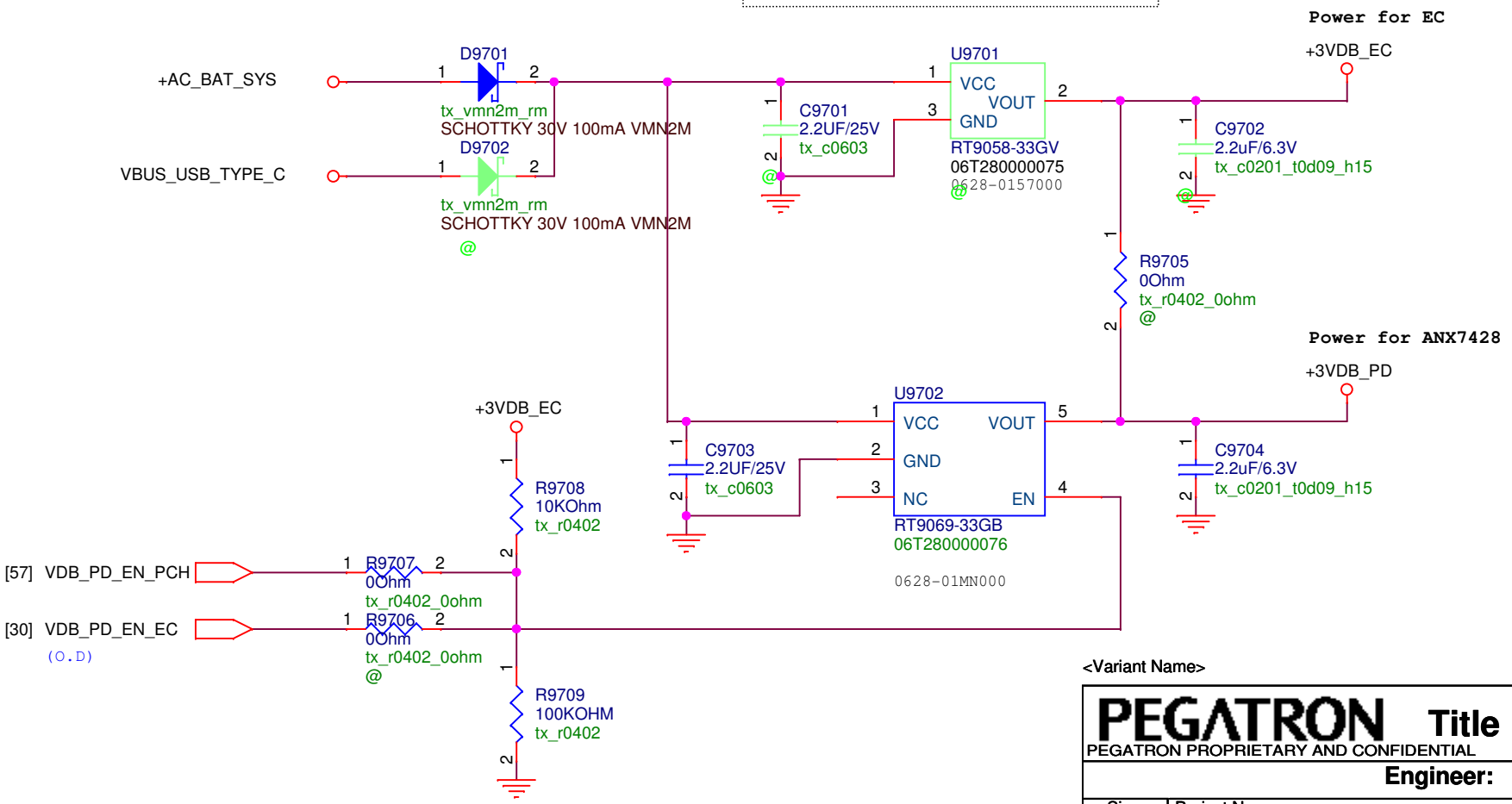
Date: Thursday, March 31, 2016 Sheet 96 of 169

Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than
5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C — VBUS_USB_TYPE_C [95,96]
+AC_BAT_SYS — +AC_BAT_SYS [45,80,81,82,83,88]
+3VDB_EC — +3VDB_EC [30]
+3VDB_PD — +3VDB_PD [95]

Requirement of U1:
1) Vin range: 4V-30V.
2) Vout: EC's operating voltage + Vf of D1
3) Output current >= EC's operating current.



<Variant Name>

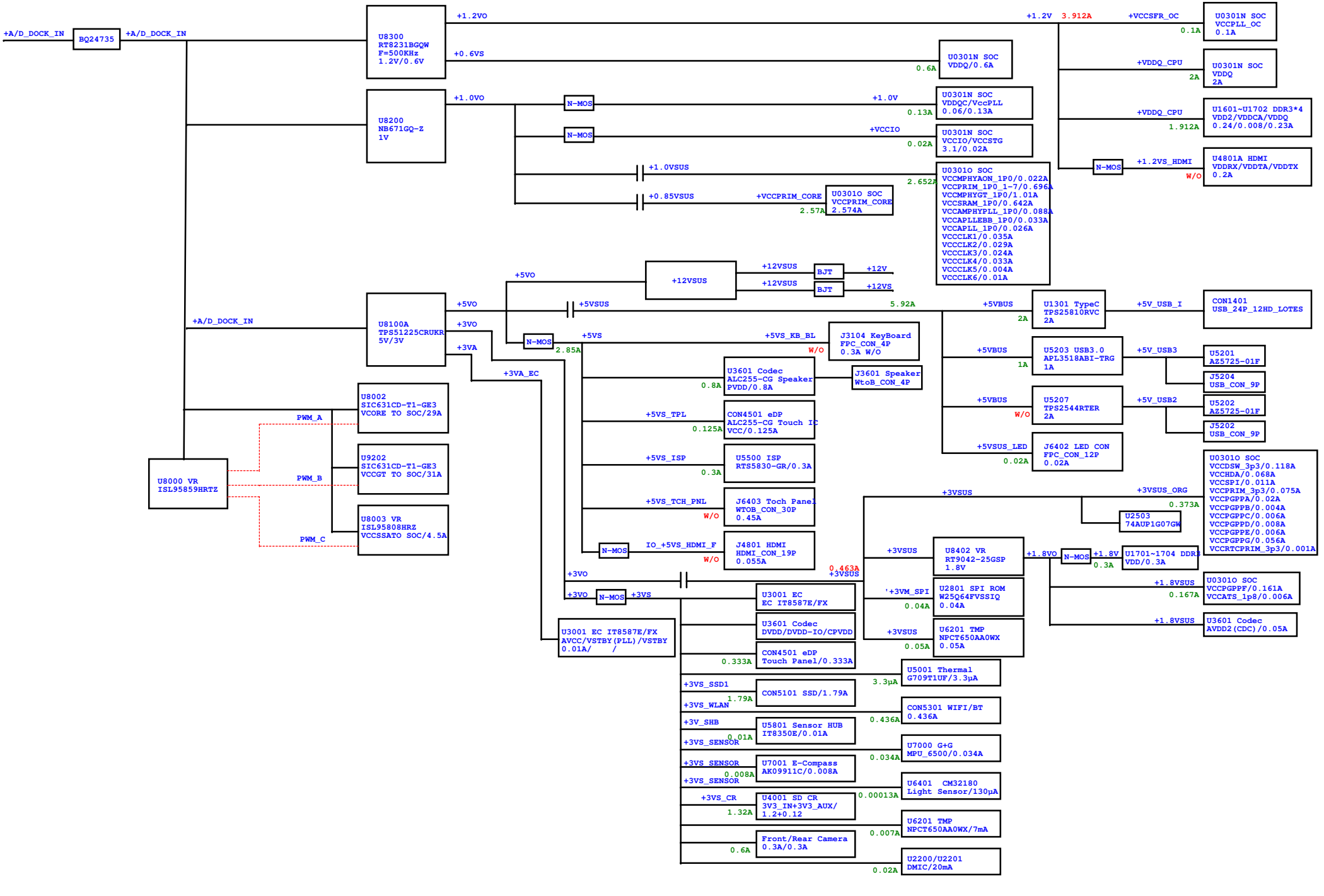
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Dead Battery

Engineer: Willy_Liao

Size	Project Name	Rev
A	HAWAII	0.0

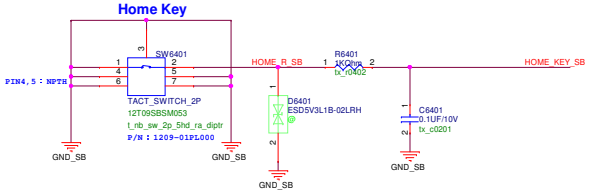
Date: Thursday, March 31, 2016 Sheet 97 of 100



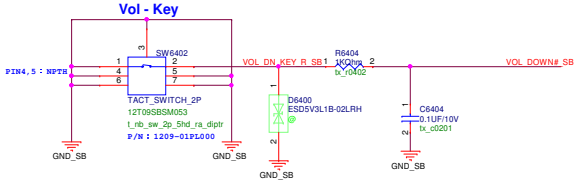
PEGATRON Title : POWER_FLOWCHART
Engineer: Tomo_Hu
HAWAII

IO Board CONN

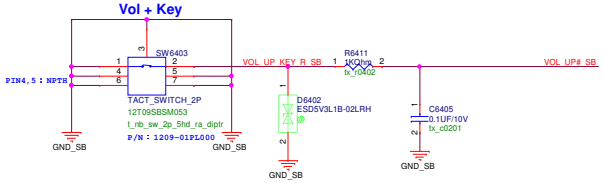
Home Key



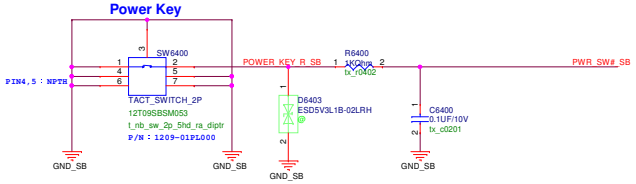
Vol - Key



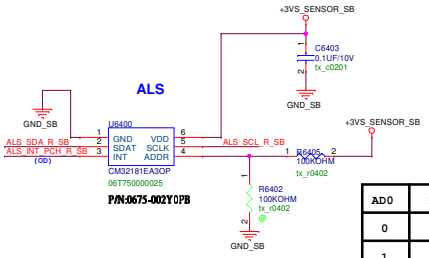
Vol + Key



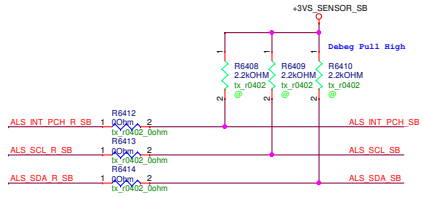
Power Key

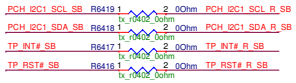


ALS

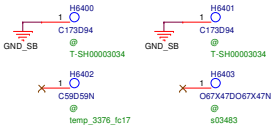


AD0	I2C Address
0	0X10
1	0X48

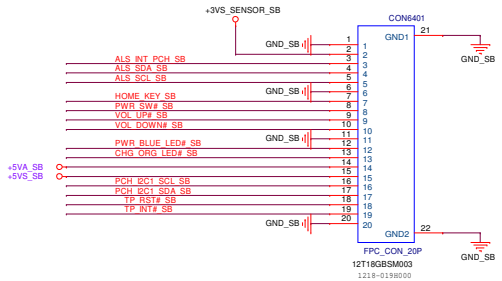


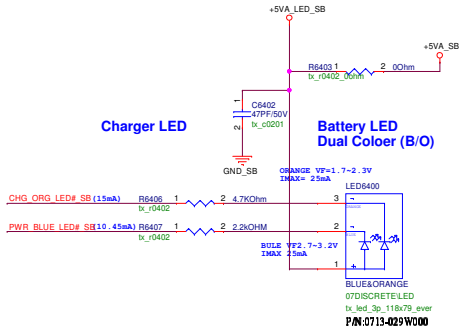


Screw Hole / Tooling Hole
(for hawaii_sub_pcb_1002)



FPC connector
(for Main PCB)

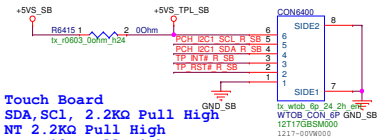




	Blue	Orange	TBD	
AC mode	Fully Charge	Charging		N/A
DC mode	100%~31%	30%~11%		10%~0%

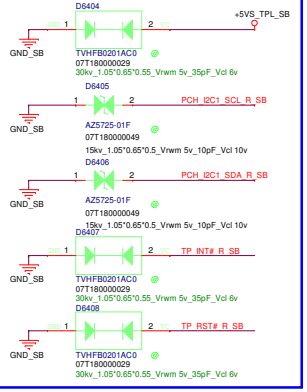
(TBD: 10%~0%,Orange)

FPC Conn.
(for Touch panel IC)



Touch Board
SDA, SCl, 2.2KΩ Pull High
NT 2.2KΩ Pull High
REST 10KΩPull High
TP SIDE PULL HIGH

Close to CON6400



PEGATRON Title : I/O Connector

BG1-NB4 Engineer: Tomo_Hu

Size	Project Name	Rev
A2	P2JCC	1.0

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